

PATTERNING AND PROCESSING OF ORGANIC ELECTRONIC DEVICES  
USING PHOTOLITHOGRAPHY

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# PATTERNING AND PROCESSING OF ORGANIC ELECTRONIC DEVICES USING PHOTOLITHOGRAPHY

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Patterning methods for chemically sensitive organic semiconductors are developed and applied to making devices and studying interesting device physics. The patterning methods developed center around industry standard photolithographic techniques, to take advantage of their high resolution, good registration and ubiquity.

First, in Chapter 2, parylene is used as a mechanically removable liftoff mask to pattern both polymers and small molecules. In Chapter 3 this technique is applied to organic thin-film transistors to pattern both the conducting polymer electrodes and the organic active region.

Chapter 4 applies the same technique to examine in detail the ionic transport of ionic transition metal complexes, which are candidates for very simple and stable solid-state lighting devices. By patterning the material, planar devices are made to resemble sandwich structure devices and a scanning probe technique can be used to see the electric field distribution of the device over time.

Chapters 5 and 6 explore the use of fluorinated solvents to make organic compatible photoresist systems capable of directly patterning organic materials. First, the solvents and resists themselves are introduced in Chapter 5 and then both individual organic transistors of high performance and organic circuits are demonstrated using these resists to structure the active layers and contacts.





### BIOGRAPHICAL SKETCH

John DeFranco was born at a very early age, in Wilmington, Delaware. He moved to California in 1986 and attended Crystal Spings Uplands Middle School and High School where he developed a love of physics from his teacher, Tom Woosnam. John pursued a Bachelor's degree at the University of California at Santa Barbara, in the College of Creative Studies with a physics concentration. He graduated in 2002 and matriculated to Cornell University in the Applied Physics PhD program. He studied with George Malliaras and defended his research in August of 2009. After that he co-founded a startup company based on his research with George, collaborator Chris Ober and Johnson school graduate Fox Holt. The company is called Orthogonal and is dedicated to commercializing the orthogonal patterning process and materials for the display industry.

To my parents.

## ACKNOWLEDGMENTS

I would like to acknowledge many people who have helped me on my journey from new grad student to this point. First, and foremost, my advisor, George Malliaras, was more than I could ask for as a mentor and a role model. Through patience and enthusiasm, he encouraged me as he did all of his group members to work hard and to have fun doing it.

Other group members helped enhance this experience and lent me their time and skills on my projects and in our collaborative work. Jason Slinker, in particular was a driving force in the iTMC projects and our collaborative work makes up a large portion of this dissertation. Dan Bernards, Matt Lloyd and Alex Mayer were invaluable for discussing ideas and in general keeping things lively. Yuanjia Zhang got me started in the clean room with my initial project (nano emitters!), which eventually led to move love of microfabrication and organic transistors.

Brad Schmidt deserves special mention as a top notch collaborator and a true friend. He got me onto my dissertation topic through our first paper together, and since then has influenced much of my career path, from choosing to minor in business to starting a company out of the research on orthogonal processing.

Also key to that area of research are several Malliaras and Ober group members who collaborated with me on orthogonal processing. Alex Zakhidov is a great researcher with a ton of device experience and a wonderful spirit. Jin-Kyun Lee is an amazingly prolific and brilliant researcher. Priscilla Taylor and Ha Soo Hwang were also instrumental in that research. And of course Chris Ober, company co-founder and photoresist guru, made a lot of this work possible.

There are many other researchers with whom I've worked over the years, and I

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## TABLE OF CONTENTS

1. Review of the Field.....	1
1.1. Introduction.....	1
1.1.1. Patterning Requirements in Organic Electronics.....	2
1.1.2. Common Methods of Patterning Organic Electronic Materials.....	5
1.1.3. Photolithographic Patterning Techniques.....	10
1.2. Photolithographic Methods for Patterning Organic Materials.....	15
1.2.1. Hybrid Techniques.....	15
1.2.2. Organic Materials Directly Processed with UV Light.....	16
1.2.3. Materials Choice or Modification.....	19
1.2.4. Patterning with an Interlayer.....	23
1.2.5. Modification of the Resist Chemistry.....	25
1.3. Conclusions and General Considerations.....	31
2. Parylene Patterning.....	35
2.1. Introduction.....	35
2.1.1. Parylene.....	36
2.1.2. Deposition Method.....	37
2.1.3. Properties.....	39
2.1.4. Characterization of parylene etch process.....	39
2.2. Subtractive Patterning of Organic Materials.....	40
2.3. Additive Patterning of Organic Materials.....	42
2.4. Film Adhesion.....	46
2.5. Film Contamination.....	47
2.6. Conclusion.....	49
3. Organic Thin-Film Transistors Made with Parylene Patterning.....	52
3.1. Introduction to Organic Thin-Film Transistors.....	52
3.1.1. Device Operation.....	52
3.1.2. Performance Parameters.....	56
3.1.3. Patterning Requirements.....	57
3.2. Peeled Electrode Devices.....	58
3.2.1. Motivation.....	58
3.2.2. Experimental.....	58
3.2.3. Results.....	60
3.2.4. Discussion.....	62
3.3. Inset Devices.....	63
3.3.1. Motivation.....	63
3.3.2. Experimental.....	63
3.3.3. Results.....	64
3.3.4. Discussion.....	64
3.4. Conclusion.....	66

4. Direct Measurement of the Electric-Field Distribution in an Ionic Transition-Metal Complex.....	68
4.1. Introduction to iTMCs.....	68
4.1.1. Comparison with OLEDs.....	68
4.1.2. Ionic Transition Metal Complexes.....	68
4.2. Kelvin Probe Measurement of Ru(bpy) Planar Device.....	69
4.2.1. Motivation.....	69
4.2.2. Kelvin Probe Microscopy.....	74
4.2.3. Measurements of Unpatterned Devices.....	75
4.2.4. Discussion.....	75
4.2.5. Patterning Ru(bpy).....	78
4.2.6. Measurements of Patterned Devices.....	80
4.2.7. Discussion.....	81
4.3. Conclusion.....	87
5. Orthogonal Processing Using Highly Fluorous Solvents.....	89
5.1. Introduction.....	89
5.2. Orthogonal Solvents.....	90
5.2.1. Orthogonal Property.....	90
5.2.2. Fluorocarbons as Orthogonal Solvents.....	91
5.2.3. Effect of Hydrofluoroethers on Organic Electronic Devices.....	92
5.3. Orthogonal Photoresists.....	96
5.3.1. Calixerene.....	96
5.3.2. FDMA-NBMA.....	101
5.4. Conclusion.....	105
6. OTFT Devices and Circuits.....	107
6.1. Introduction.....	107
6.2. Applications to Organic Transistors.....	107
6.2.1. Top Contact vs. Bottom Contact OTFT Architectures.....	107
6.2.2. Experimental.....	110
6.2.3. Results.....	111
6.2.4. Discussion.....	113
6.3. Ring Oscillator Circuits.....	113
6.3.1. Smooth Gold for Gate Electrodes.....	114
6.3.2. Al <sub>2</sub> O <sub>3</sub> Gate Dielectrics Deposited by ALD.....	114
6.3.3. Pentacene Transistors Using Thin Al <sub>2</sub> O <sub>3</sub> Gate Dielectric.....	117
6.3.4. Design and Fabrication Considerations.....	117
6.3.5. Results.....	119
6.3.6. Discussion.....	119
6.4. Conclusion.....	121
7. Summary of Conclusions.....	123
References.....	124

## LIST OF FIGURES

Figure 1.1 OLED microdisplay showing high-resolution patterning.	4
Figure 1.2. Laser-Induced Thermal Imaging (LITI) process.	7
Figure 1.3. (a)–(c) Small molecule patterning by organic vapor jet printing, with penny for scale. (d) Schematic of OVJP apparatus.	11
Figure 1.4. (a) Subtractive patterning using photolithography. (b) Liftoff or additive patterning.	13
Figure 1.5. The use of polyimide dewetting layers to facilitate the inkjet patterning of PEDOT:PSS to form source/drain electrodes.	17
Figure 1.6. Fabrication of full-color displays using cross-linked emitters.	18
Figure 1.7. (a)–(h) Process for making a full-color display with a cross-linked PEDOT:PSS layer used as a buffer layer. (i) Resulting image of one-color device.	21
Figure 1.8. OLED stack patterned with an SU-8 liftoff procedure.	22
Figure 1.9. AFM image of pentacene patterned using a parylene liftoff process.	26
Figure 1.10. $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ device operating in a beaker of boiling HFE solvent.	30
Figure 1.11. Photoluminescence of cross patterns of two different light emitting materials, patterned using calixerene liftoff patterning. The blue line is a polyfluorene and the red is $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$	32

Figure 2.1. The parylene process: (a) Starting with the dimer molecule, the parylene goes through a pyrolysis process to be turned into the monomer form (b), before polymerizing at room temperature on the substrate surface (c).	38
Figure 2.2. (a) Subtractive parylene patterning process. (b) Additive or liftoff parylene patterning process.	43
Figure 2.3. (a) and (b) show trenches etched in PEDOT:PSS using the subtractive parylene patterning technique. (c) PEDOT:PSS and (d) $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ patterned with the additive technique.	45
Figure 2.4. SEM image showing spike formation in the trench between two gold electrodes. Image is taken after coating with $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ .	48
Figure 3.1. Typical OTFT device architecture.	53
Figure 3.2. (a) Device made using the peeled electrode parylene technique. (b) IV characteristics for the $2\mu\text{m}$ channel device with pentacene electrodes.	61
Figure 3.3. (a) Completed inset device. (b) IV curve of device.	65
Figure 4.1. $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ diagram and energy levels of HOMO and LUMO.	70
Figure 4.2. Diagram of EFM experiment and comparison of two models.	73
Figure 4.3. (a) Potential across unpatterned device. (b) Electric field. (c) Potential near anode.	76
Figure 4.4. Diagram of patterned vs. unpatterned devices under bias.	77
Figure 4.5. Process flow for patterned planar devices.	79
Figure 4.6. Peeling of parylene layer from the electrode with tweezers.	82



Figure 4.7. (a) Potential across patterned device. (b) Electric field. (c) Potential near anode.	83
Figure 4.8. (a) Voltage drop at steady state for different applied biases. (b) Electric field. (c) Light emission profile across device. Left side is anode, right side is cathode.	85
Figure 5.1. Chemical structure for (a) HFE 7100 and (b) HFE 7500.	92
Figure 5.2. (a) Gate sweeps of P3HT devices before and after exposure to solvents. (b) Performance of $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ device with solvent exposure. (c) $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ device operating in boiling HFE solvent.	94
Figure 5.3. Calixerene molecule and synthesis process.	98
Figure 5.4. (a) Schematic of PAG. (b, c) Images from optical lithography. (d) E-beam patterns.	100
Figure 5.5. (a–c) Lithographic patterns in FDMA-NBMA. (d) E-beam patterns.	104
Figure 6.1. (a) Top source-drain electrodes on pentacene. (b) IV curve.	112
Figure 6.2. AFM of gold surface with an RMS roughness of 0.7 nm.	116
Figure 6.3. Ring oscillator based in 1 $\mu\text{m}$ long channel Pentacene OTFTs. (A) Optical microcopy image of ring oscillator based on Pentacene TFTs. (B) Output characteristic of the device at $V_{DD} = -55\text{V}$ .	120



## LIST OF TABLES

Table 5.1. The results of solvent treatment on P3HT OTFTs and $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ electroluminescent devices. The data represent changes in the field-effect hole mobility of the former and the quantum efficiency of the latter after solvent treatment.....	95
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## CHAPTER 1

### REVIEW OF THE FIELD

#### ***1.1 Introduction***

Over the course of the development of the field of organic electronics[1], patterning has played an increasingly important role. Early work was focused on materials properties, such as charge transport[2], charge injection, luminous efficiency and film growth[3]. All of these parameters are still very important, especially in the new materials that are continually being developed. A new emphasis has been placed, however, on device architecture and manufacturability on greater-than-lab scales. The move from single organic light emitting diode (OLED) devices[4] to pixelated displays, from single large organic thin-film transistors[5] (OTFT) to circuits and display backplanes[6], and from small organic photovoltaic devices[7] (OPV) to large-area, fault tolerant architectures, has necessitated advances in patterning numerous layers, with both organic and inorganic materials compositions.

While a variety of methods for patterning these organic materials have been developed, there has been steadily increasing interest in using methods that are already well established in the semiconductor manufacturing industry, namely photolithography. Several reviews have covered organic patterning methods previously [8–9] [Some have mentioned methods of photolithography applied to organic electronics as a side note, but none to date have attempted a focused review. This chapter will cover some of the requirements and popular methods of patterning

organic electronic materials, giving special attention to the use of photolithography in patterning a range of organic electronic devices.

### **1.1.1 Patterning Requirements in Organic Electronics**

OFTFs make use of patterning in many steps of fabrication. The most obvious and important use of patterning is in defining source and drain contacts, hence the transistor channel. Channel length and width, or more specifically the ratio of the two, helps determine the drain current of a transistor. The degree to which the patterning technique can decrease  $L$  while maintaining a reasonable width (given the space requirements) the better performing the transistor will be. The natural limit of this scaling is set by the contact resistance, since ohmic contacts might become injection limited at small channel lengths[10]. However once proper metal/organic semiconductor interface is chosen this length may be as small as 30 nm[11].

The source-drain electrodes are not the only layer requiring patterning in organic TFTs. Preventing leakage between source and drain through ungated material, or even between devices, requires that the active layer is patterned and material is removed from regions far from the channel. Patterning the organic semiconductor typically leads to the enhancement of on-off ratio, as parasitic current is minimized when no gate voltage is applied.

The need for patterning in OLEDs for use in displays and signage necessitates the definition of the individual pixels and sub-pixels. The resolution requirements for display pixels vary widely, depending on the screen size, resolution and sub-pixel

architecture. Television displays might have pixel pitch of 80 $\mu$ m, with sub-pixels around one third of that. OLED microdisplays[12] often have  $\sim$ 12  $\mu$ m pixel pitches in order to get full screen resolution into a sub- 1-inch diagonal display (Figure 1.1). Displays meant for signage naturally have much large pixels than either of these.

The needs for patterning are greatly reduced in the cases of lighting and photovoltaic devices. Such devices are meant to cover large areas and don't require pixelation. Some sort of segmentation might be required, however, in order to give the systems fault tolerance for defects in the film and to tune the input/output characteristics.

There are a variety of organic electronics based sensors[13], from OLED based devices that utilize the absorption spectra of target molecules, to conducting polymer based sensors, which detect changes in doping level from an analyte in solution[14]. Since the architectures are similar to other organic electronic devices, the pattern needed can be much the same. The levels of integration with other elements, such as microfluidic channels, can make patterning decisions more crucial[15].

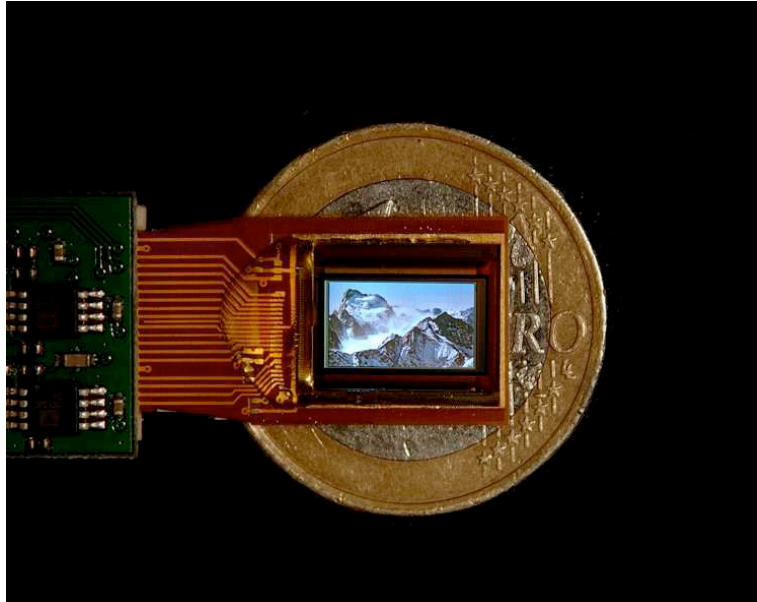


Figure 1.1 OLED microdisplay showing high-resolution patterning.

### **1.1.2 Common Methods of Patterning Organic Electronic Materials**

#### ***Solution-Deposited Materials***

One of the advantages of solution processed materials, whether polymer or small molecule, is the ability to use drop-on-demand delivery to allow simultaneous deposition and patterning of active layers. Inkjet printing of organic TFTs has been demonstrated where the source-drain electrodes and active region have been patterned or where all layers, including the gate and gate dielectric are printed with inkjet[16].

Inkjet printing is also of potential importance to the display industry[17]. All of the necessary layers needed for an OLED stack can be printed, making it possible to produce three-color active matrix displays using only inkjet, and in fact some companies like Cambridge Display Technologies are pursuing that route commercially. For inkjet printing to work, specially formulated inks must be made from the various solution-processable polymer and small molecule electronic materials available. It takes a lot of effort to produce inks that have the proper rheological properties to print and still have good performance as organic semiconductors. Lifetimes of printable OLED materials are still lagging behind vacuum-deposited same-color equivalents, but are catching up, and some printable small molecules are there already.

A wide variety of printing methods that have analogs in graphic arts printing have been modified to be used with organic electronic materials. The speed at which the roll-to-roll printers pattern inks, is no doubt the biggest motivator in using printing for



electronics manufacturing. High throughput would undoubtedly lead to low cost devices, provided the functionality remains adequate.

Laser patterning can be used with organic materials, subtractively as an ablation tool[18–20], as a means to change the chemical properties of the deposited film or additively. The second method can take different forms. Abdou and colleagues[21] used a laser to crosslink regions of a P3HT film, rendering it insoluble to the chloroform/acetone solvent mixture used to remove the unexposed regions. The film was then doped with nitrosonium tetrafluoroborate or ferric chloride, creating conducting lines. The exposed region of organic material may also be rendered non-conducting through laser-induced photobleaching[22], for transistor isolation. Additive laser patterning, where material is moved from a donor film to the substrate through local laser heating, is currently a top candidate for large area OLED displays. The laser induced thermal imaging (LITI) process consists of laminating a solution coatable transfer sheet to a substrate, imaging the patterns with a laser to transfer the material and then peeling off the sheet from the substrate. Multiple layers can be simultaneously transferred, and the materials can be polymers or small molecules. Blanchet et al.[23] used this technique to pattern conducting polymers for organic TFTs (Figure 1.2). Other similar techniques that do not require direct lamination include radiation induced sublimation transfer (RIST), which uses an 810 nm laser to locally heat the material, and laser induced local transfer (LIST), in which an IR absorber is heated with a 1064 nm laser.

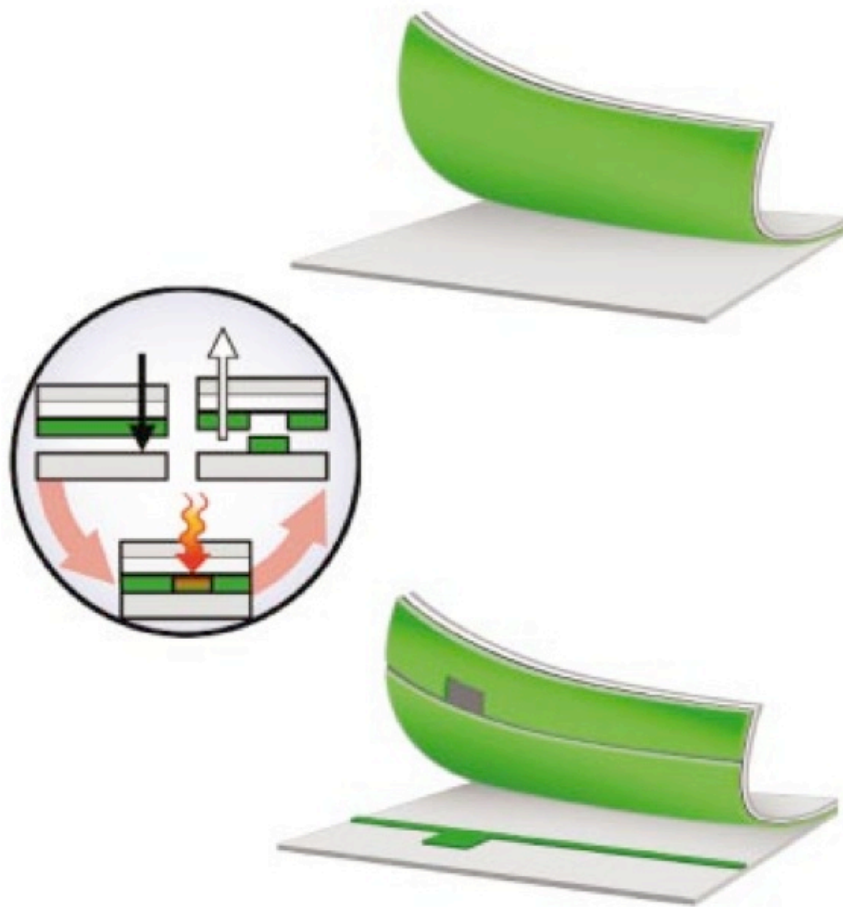


Figure 1.2. Laser-Induced Thermal Imaging (LITI) process.

Physical pattern transfer from a stamp is another major area of micropatterning that may be applied to organic electronics patterning. Using a hard mask to transfer a pattern into resist or active layer is known as nanoimprint lithography[24]. The mask can be any hard material—though usually silicon or glass—that is patterned itself with lithographic methods, including photolithography and ebeam lithography. The latter allows for resolutions less than 100 nm that are faithfully reproduced in the underlying film, making this technique one of the highest resolution possible. Kao et al. applied this method[25] to make OLED devices, demonstrating not high resolution, but rather reproducible, fairly large area patterning.

The more common approach to stamping in organic electronics is the use of soft elastomeric stamps to transfer materials onto a substrate (an excellent overview can be found in reference [8]). Inorganic materials[26], resist[27–29] and organic materials may be patterned with these techniques. Examples of the latter include patterning light emitting materials[30, 31] and photonic crystals for making organic lasers[32]. Another important use is in depositing electrodes onto an elastomeric stamp and then laminating the stamp onto organic devices, thus avoiding damage from metal deposition[33] and make small, high-performance transistors[34]. It is also possible to laminate two organic layers together, to form interfaces that would otherwise be difficult or impossible to fabricate[35].

### ***Vapor-Deposited Materials***

The simplest and lowest cost method to pattern vapor-deposited small molecules on a small scale is the use of a shadow mask. The method involves etching holes in a thin piece of metal, which is used to selectively block the passage of molecules during the deposition process. Shadow masking is used extensively in industry to make OLED displays for cell phones on substrates up to ~1 m (gen 4.5). It may be difficult to scale the method much beyond this, however, because of the difficulty of working with large, thin sheets of metal. In the first place, sagging becomes an issue at these larger sizes, unless substrates are held vertically (which most now are). It is also a problem that dust can break off and contaminate the substrate if the mask is allowed to flex too much. Further, handling and cleaning of the masks can be expensive and cumbersome at larger sizes. Shadow masking does have the benefit of producing the highest performing OLED devices because all deposition can be done while in vacuum and no chemicals touch the organic materials before encapsulation. Shadow masks are widely acknowledged as a stop-gap technology that works now, but will need to be replaced if the industry is to reach larger substrates and production volumes. In principal deposition through shadow mask (also sometimes referred as stencil lithography) can be very high resolution and give features of down to 10 nm scale[36], however commercial application so far is limited to low resolution features due to problems mentioned above.

Organic vapor jet printing[37] was developed in order to bring the deposit-on-demand nature of inkjet printing to materials that are normally deposited in vacuum. The technique is a printing version of a deposition technique called organic vapor phase

deposition[38] that involves using an inert carrier gas to create a steady, laminar flow of the deposited material (Figure 1.3). Besides enabling the patterning of small molecules with high resolutions, the carrier gas deposition method gives greater control over deposition conditions, including rate, morphology and materials interfaces, than sublimation. Improvements to materials performance with this method have been reported[39].

### **1.1.3 Photolithographic Patterning Techniques**

Photolithography is the nearly ubiquitous method of patterning thin films by using a layer that can be patterned using selective exposure of UV light, generally through a pre-formed photomask with a pattern on it made of chrome, and then developed leaving either the exposed material (negative tone resist) or unexposed material (positive tone resist) behind to control the next processing step. Once patterned, resist can be used to shield material beneath it from an etchant, so that only uncovered materials are etched (subtractive patterning). Alternatively, the resist can be used as a contact mask to pattern a deposited layer (additive patterning). Figure 1.4 shows both processes step by step. Subtractive etching is far more common in the silicon industry, since fast, selective etchants are available for most materials and liftoff itself can leave residue. On the other hand, certain materials, platinum for example, are usually patterned with a liftoff method.

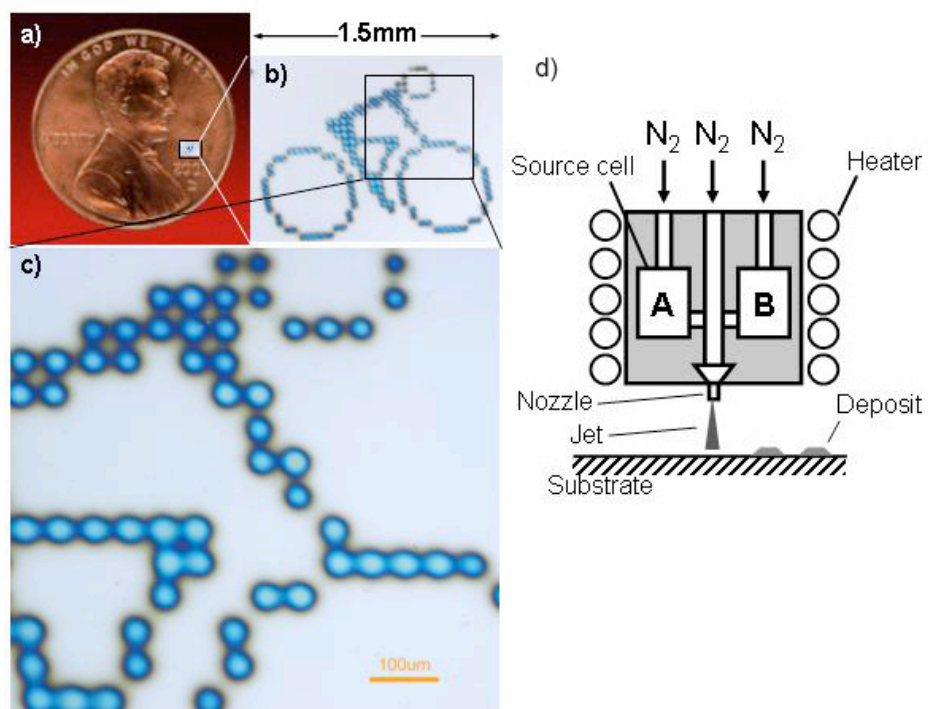


Figure 1.3. (a)–(c) Small molecule patterning by organic vapor jet printing, with penny for scale. (d) Schematic of OVJP apparatus.

The advantages of photolithography are numerous. It is an extremely high-resolution process, capable of producing features  $< 32$  nm (current manufacturing), with that figure improving almost yearly[40]. Through the development of large-scale LCD manufacturing[41], large area substrates ( $> 2$  m on a side) can be processed and since it is a parallel process (many features exposed at one time), the time to pattern a large substrate is less than a minute, making throughput relatively high (though clearly not as high as the high-speed printing techniques). A key advantage is in overlay, where one layer can be precisely and accurately ( $< 0.1$   $\mu\text{m}$ ) placed on another layer, a difficult task with many alternative techniques. Lastly, but perhaps most importantly, there is a large installed base of equipment and trained engineers. This is an important fact for the commercialization of a new technology, because startup costs can be much higher starting from scratch.

The major hindrances in applying the techniques of photolithography to patterning organic electronic materials have been twofold. The first reason is cost. For some time, the field of organic electronics has been focused on low cost fabrication in order to compete with traditional semiconductors on price, if not on performance. Photolithography has been seen as a high cost method, due to the large investments necessary for capital equipment and low throughput. Very few papers have looked into the real manufacturing costs of these various techniques, as they would be used at scale.

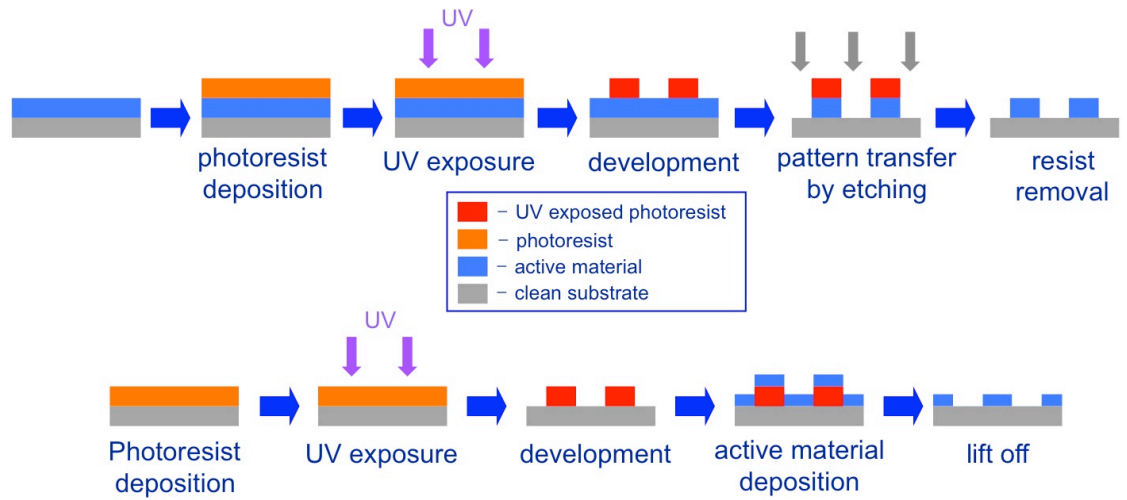


Figure 1.4. (a) Subtractive patterning using photolithography. (b) Lift-off or additive patterning.



Sheats[42] did a comparison study for a variety of manufacturing techniques used in current semiconductor manufacturing and proposed for organic processing, presenting a convincing argument that printing techniques such as inkjet are not inherently low-cost, at least when compared to high volume photolithographic patterning.

A second reason that photolithography isn't widely used is the general difficulty of working with solvents and developers that tend to damage the active materials being patterned. There are many varieties of photoresist available, but diazonaphthoquinone sensitized phenol formaldehyde resin (DNQ- novolak) is a very common formulation, used for mercury arc lamp sourced photolith tools (wavelengths between 436 nm g-line and 365 nm i-line). DNQ-novolak is typically deposited from propylene glycol monomethyl ether acetate (PGMEA), a generally mild solvent that is nevertheless capable of damaging organic thin films. Most of the process damage, however, comes from the tetramethyl ammonium hydroxide (TMAH) developer. The developer is water based and a strong caustic, both very bad for semiconducting organic films. Water alone has been studied extensively as the cause of degradation in OLEDs[43, 44] , OTFTs[45–47] and OPVs. Removal of the resist after processing uses stronger organic solvents than the one used for deposition; acetone is common. Most organic electronic materials do not survive the process (they dissolve, crack, delaminate, etc), or perform very poorly afterwards.

Photolithography has been used in device fabrication for patterning certain layers in OTFT devices, specifically metal for source-drain electrodes for bottom contact

transistors. All of the processing in that case takes place before the active organic material is introduced and so solvent damage is avoided. There are some limitations to making devices this way, namely mobility and charge injection for bottom contact devices suffer, unless special tricks are used[48]. But photolithography has not been applied as widely to the patterning of the active layer or subsequent layers.

## ***1.2 Photolithographic Methods for Patterning Organic Materials***

### **1.2.1 Hybrid Techniques**

Photolithography has been used in combination with other techniques in order to mitigate their shortcomings, whether those are reproducibility or resolution and registration. These hybrid techniques usually use photolithography early in the process in order to introduce pre-patterns, avoiding any possible chemical damage during the later deposition process.

Shadow masking has limitations, as was mentioned earlier, in high-resolution patterning (less than 100 $\mu$ m line spacing) and registration. This is a problem for high resolution patterning of cathode layers on top of OLEDs for passive matrix displays. One way to improve this is to include an additional layer of patterned photoresist in order to act as an integrated mask[49].

Another hybrid technique is the use of photolithographically patterned polymer films to modify the wetting properties of the substrate surface to enhance inkjet printing. In order to overcome deficiencies in the achievable resolution of inkjet printing, surface energy patterning was used to form channels for polymer TFT electrodes. Sirringhaus and coworkers used photolithographically patterned polyimide

along with inkjet printing of PEDOT:PSS to form OTFT channels with 5  $\mu\text{m}$  channel length[50] (see Figure 1.5), far below what ordinary inkjet printing would allow ( $>20 \mu\text{m}$ ). Further improvements have pushed that length to 250 nm[51], and below [52] although stamping and not lithography was used in those cases.

### **1.2.2 Organic Materials Directly Processed with UV Light**

Taking advantage of the chemical tunability of organic materials, direct patterning by exposure to UV has been used by many to create devices. The advantage of this method is that no other layers are needed to transfer the pattern into the material, potentially saving on materials costs.

Photo-induced cross-linking was used by Müller and coworkers[53] to make oxetane functionalized light-emitting spiro-bifluorene-co-fluorene polymers that behave like negative photoresists. The specific mechanism involved a photoacid generator (PAG), specifically (4-[(2-hydroxytetradecyl)oxyl]phenyl) phenyliodonium hexafluorantimonate, that produces a proton when activated by UV light. The oxetane ring of the precursor is opened and this initiates the chain polymerization, cross-linking the material. Full-color displays[54] were demonstrated with this method, as shown in Figure 1.6. Similarly, hole transport layers (HTL) cross-linked with oxetane side-groups were developed by Bacher et al.[55], with bis(diarylamine) used as the HTL.

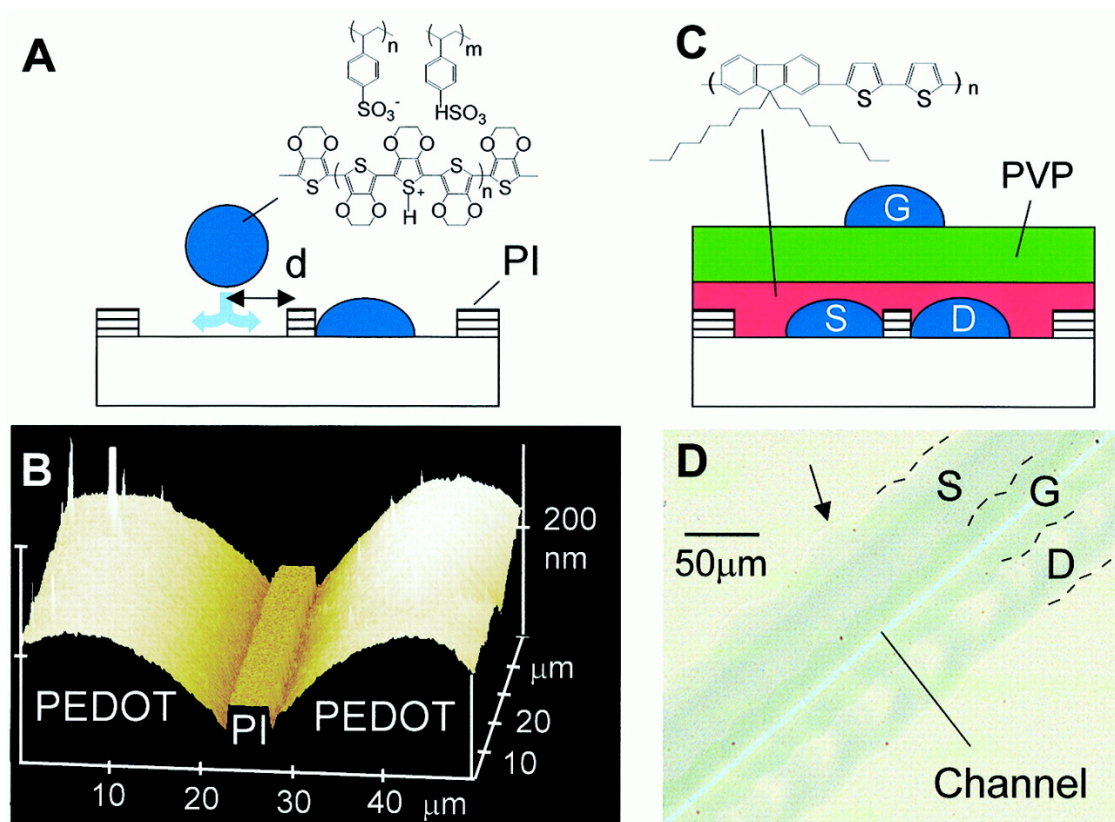


Figure 1.5. The use of polyimide dewetting layers to facilitate the inkjet patterning of PEDOT:PSS to form source/drain electrodes.

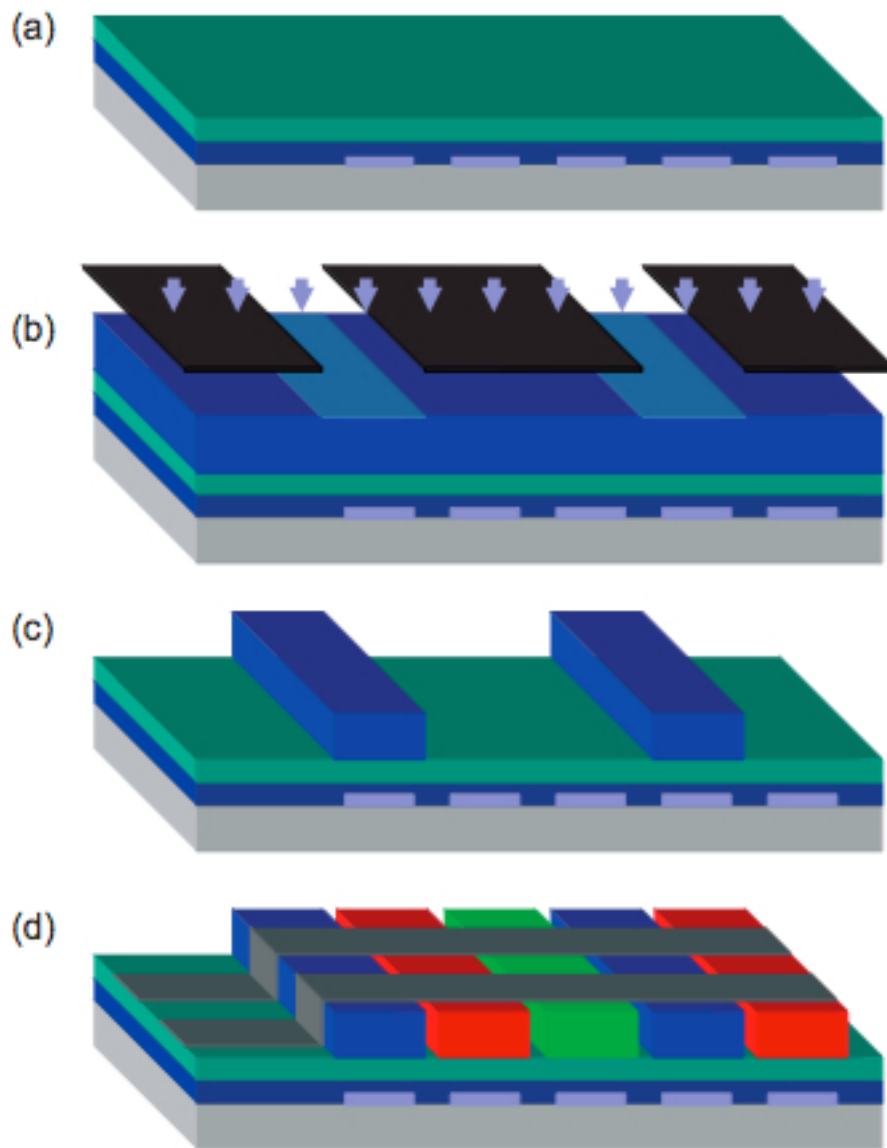


Figure 1.6. Fabrication of full-color displays using cross-linked emitters.

Solomesch and coworkers[56] extended this concept to use crosslinkable triarylamine photopolymers as binders for higher efficiency light emitting materials, in this case PPV derivatives. Triarylamine was chosen because it was chemically compatible with the light emitting polymer, and had a higher bandgap to prevent quenching and charge trapping.

Another example of successful utilizing of this concept was shown by Afzali and co-authors[57], who fabricated photopatternable pentacene precursor for OTFT application.

The conducting polymer PEDOT has been used with a variety of patterning techniques, including photolithography. Selectively crosslinking PEDOT using a photoinitiator and UV light, can turn PEDOT:PSS into a kind of negative-tone photoresist, as was demonstrated by Touwslager and coworkers[58] in the fabrication of organic code generators. This is because the film is nearly insoluble once cast as a thin film. The common form of PEDOT:PSS, which is spin-coated from a water solution is actually only a suspension. It can become delaminated during the development stage, however and the film integrity may be compromised during a standard photolithographic process. Using cross-linking agents, the PEDOT layers, and in some cases the layers placed on top, can be made impervious to delamination during processing[59] (Figure 1.7).

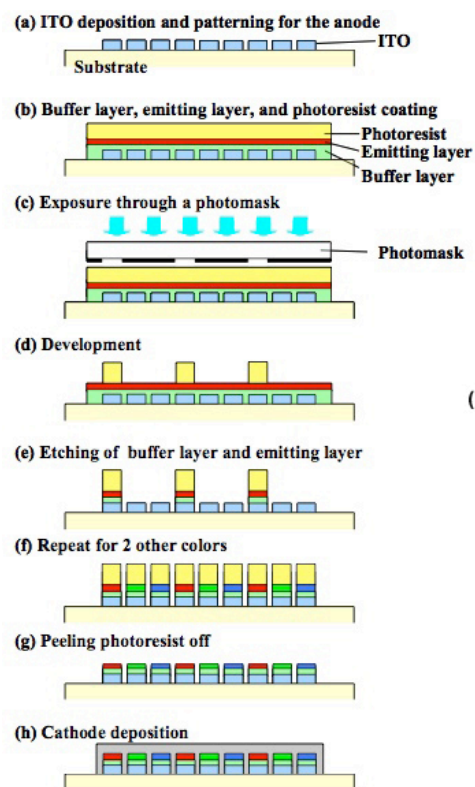
### **1.2.3 Materials Choice or Modification**

Certain organic electronic materials, some with structural modifications, can be used with standard photolithographic processes. Polymeric materials are usually more robust to chemical damage from photolithography.

An example of successful patterning using photolithography is the demonstrated by Huang and coworkers[60]. SU-8, a negative tone photoresist is used to pattern the emitting layers. Stacks of polymer OLED materials are selectively removed through a liftoff process during development of the resist (Figure 1.8). Since the developer used is PGMEA, a relatively mild organic solvent, little damage occurs and multiple layers can be patterned in this way.

A downside to this method is that the SU-8 remains under the stack, which can diminish the optical transmission (reported as 80% in the visible spectrum) and block electrical connection to the substrate.

Careful choice of active material can allow direct patterning with more common types of photoresist. In a very early example[61], metal is patterned on top of poly (2,5-dialkoxy-p-phenylene- vinylene) (PDAOPV) a PPV derivative. It was found in that experiment that the most damaging step was baking the light emitting polymer, not dipping it in chemicals. Regioregular polythiophene (P3HT) has been successfully patterned directly using standard photoresist chemistry, using both liftoff[62] method and etching[63].



(i)

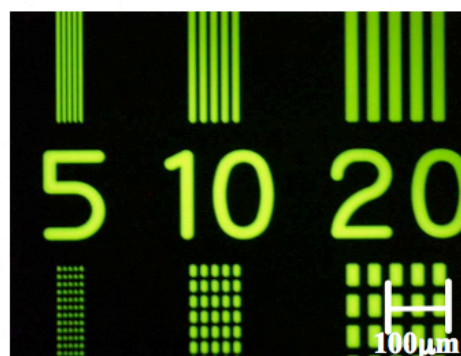


Figure 1.7. (a)–(h) Process for making a full-color display with a cross-linked PEDOT:PSS layer used as a buffer layer. (i) Resulting image of one-color device.



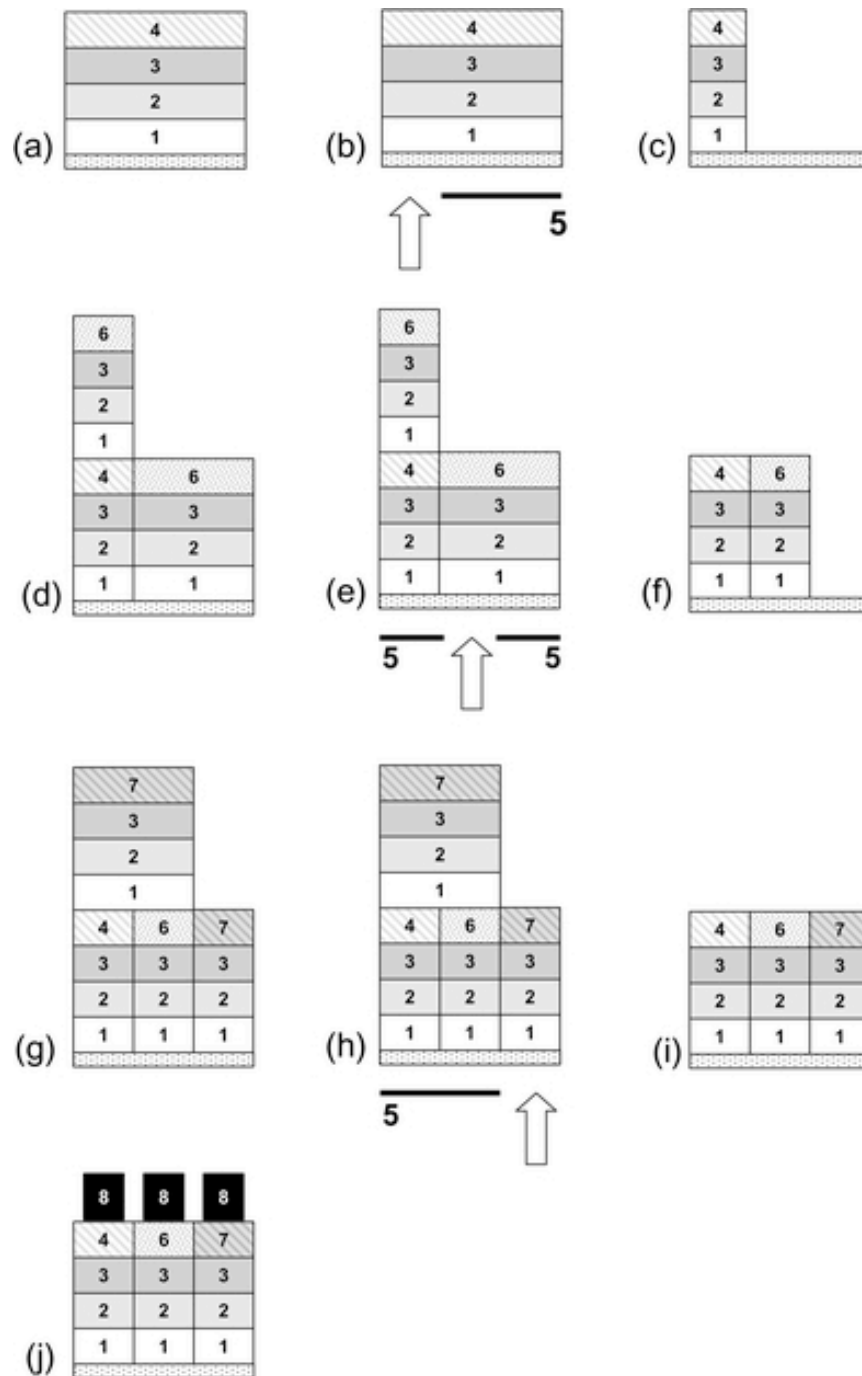


Figure 1.8. OLED stack patterned with an SU-8 liftoff procedure.

#### 1.2.4 Patterning with an Interlayer

Perhaps the most popular way to avoid contact between the harsh chemicals used in photolithography from making contact with the active layer of an organic device, is to use an inert, protective interlayer. The properties of such a layer must include a benign deposition process, low etch rates in the solvents used in photolithography, low permeability to those same solvents and the ability to be selectively etched in another way, usually by oxygen plasma RIE. Removal of the material after patterning is usually optional, as the protective layer may double as an encapsulant in many cases.

Parylene is often used in this kind of process. It is an inert polymer that is deposited through a room temperature chemical vapor deposition process. The material itself is nearly impervious to chemical attack, showing no appreciable etch rate in most organic solvents or even strong acids. The conformal coating property of the film allows it to effectively encapsulate the entire substrate while further processing occurs, preventing lower layers from exposure to solvents and aqueous developers. It etches easily in oxygen plasma, which allows facile patterning of lower organic layers with minimal undercutting.

Kymissis et al.[64] have demonstrated subtractively patterned pentacene transistors using parylene and oxygen plasma. DeFranco et al.[65] showed a similar technique on a wider range of organic materials, using parylene to pattern electrodes made of PEDOT:PSS with narrow channels. Features as small as 1  $\mu\text{m}$  were patterned on  $\text{SiO}_2$  substrates.

Polyvinyl alcohol (PVA) is a spin-coatable water-soluble material that is also commonly used for this kind of process[66]. Zhou et al.[67] used photosensitized PVA to pattern pentacene TFTs for an active matrix flexible display. Other organic circuits have been made in a similar fashion[68].

Inorganic oxide layers have been used as hard etch masks as well, with the additional benefit of serving as dielectric layers for top gated TFTs. Li and coworkers [69] used silicon nitride (SiN) deposited with plasma enhanced chemical vapor deposition (PECVD) as a protective hard mask and gate dielectric on top of P3HT transistors. Chang et al.[70] demonstrated that atomic layer deposition (ALD) deposited aluminum oxide allowed for photolithographic patterning of MEH-PPV based OLEDs. In both cases, the layers were left intact and used for another purpose, which is necessary in such a scheme because of the inability to later remove the layer without damaging the rest of the device.

Metal can also be quite an effective encapsulant[71], and in the case of OLEDs, this metal layer can double as a top electrode. Tian et al.[72] used a thick metal layer ( $>1\mu\text{m}$ ) to protect a vacuum deposited OLED from process conditions, allowing three side-by-side OLED pixels to be patterned even though harsh chemical etchants were used, including hydrofluoric acid. Lamprecht et al.[73] used a thinner (150nm Aluminum) metal barrier to protect an OLED/OPV stack from a photoresist-masked subtractive etch.

Materials that can be effectively removed from the substrate without the use of solvents can be used to lift off an organic material in order to pattern it. In this way the

technique shares some features with stamping; controlling the surface energy between different materials so that sacrificial layer releases from the substrate, but the patterned organic material remains stuck to the surface. DeFranco et al.[65] demonstrated that the parylene layer shows poor adhesion to the surface of an oxide coated silicon wafer and so can be peeled from that surface to allow for mechanical dry liftoff of a variety of polymers and small molecules (Figure 1.9). Other materials besides parylene can also be used for this purpose, for example Chang and Sirringhaus showed a similar delamination method with polyimide[74]. Patterning of polyimide does not require oxygen plasma etching, since it dissolves in the developer used on the top lying photoresist. That developer, however, might damage lower layers, potentially limiting multilayer patterning. This of course is a limitation of most interlayer liftoff techniques, because they seek to avoid damage by using all of the damaging chemicals before the organic layer is deposited. If other layers are there first, then this strategy doesn't work as well.

### **1.2.5 Modification of the Resist Chemistry**

One final method of protecting the organic layers from chemical damage from resist processing is to change the chemicals used in the photolithography process itself. Two recent examples of this approach are resist materials processed with supercritical fluids and those processed with highly fluoruous solvents.

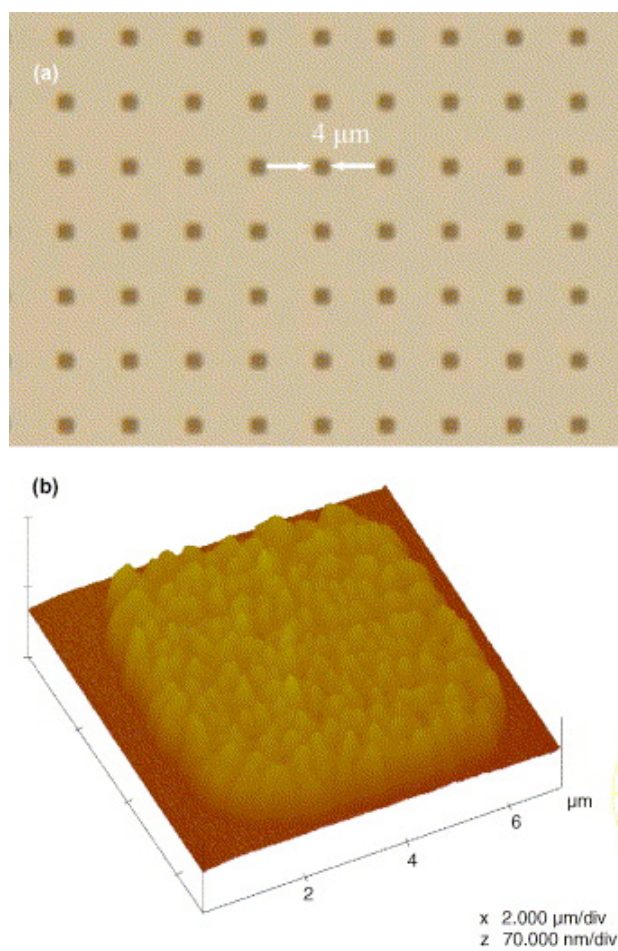


Figure 1.9. AFM image of pentacene patterned using a parylene liftoff process.

In order to be completely benign to the layers being patterned, all of the harmful chemical steps must be eliminated, including deposition, development and stripping (lift off), since each contributes to damage. Once this is accomplished, a truly simple method of patterning is achieved, so that organic electronic materials can be treated in much the same way as any inorganic material.

Super critical carbon dioxide (scCO<sub>2</sub>) is a phase of carbon dioxide raised to a pressure and temperature past its critical temperature and pressure ( $T_c = 31.1^\circ\text{C}$ ;  $P_c = 73.8$  bar). ScCO<sub>2</sub> has high diffusivity and zero surface tension (which is important for high aspect ratio features as well as extremely small features), and has proven to be an excellent solvent in dry lithography for high resolution nano-fabrication. Another very important aspect is that scCO<sub>2</sub> is a non- toxic, non-inflammable, environmentally friendly fluid, which is proposed as a key driver in the new field of “green” chemistry [75]. In recent years scCO<sub>2</sub> is being considered as a low-cost substitute solvent in microelectronics processing such as wafer cleaning, spin coating, etching, and resist stripping, based on its physical and chemical advantages[76]. Besides these general advantages, the fact that scCO<sub>2</sub> is a poor solvent for most ionic, high molecular weight and low vapor pressure organic compounds makes it an extremely promising a non- destructive development medium for the vast majority of materials utilized in organic electronics. Essential to this patterning approach is the ability to develop the photoresist without harming the active organic material. Based on the high affinity of scCO<sub>2</sub> for fluorocarbons, it has been demonstrated that appropriate statistical copolymers with high fluorine content are effective negative photoresists for

development with scCO<sub>2</sub>. Another important advantage of the fluorinated polymers is their hydrophobicity and oleophobicity, i.e. they repel and/or resist both water and most organic solvents. Moreover, for those types of materials one can use a high fluorine content solvent (trifluorotoluene, hydrofluoroethers, etc.) with essentially the same properties.

Similar to scCO<sub>2</sub>, highly fluorinated liquids, in general, do not interact with non-fluorinated materials. It is thus anticipated that those fluids will extend the options for solvent orthogonality. Among the various fluorinated solvents, hydrofluoroethers (HFEs) are particularly attractive because they are environmentally friendly, non-toxic, non-flammable and non-ozone depleting solvents[77].

To establish HFEs as universal processing media, possible deterioration of the performance of organic electronic devices in these solvents was investigated by Zakhidov et al.[78] Poly-3-hexylthiophene (P3HT), a prototypical conjugated polymer soluble in non-polar organic solvents, did not show any performance variation in terms of field-effect mobility after extensive exposure to HFEs. The benign nature of HFEs was further demonstrated in an experiment where OLEDs prepared with poly(dioctylfluorene) and [Ru(bpy)<sub>3</sub>]<sup>2+</sup>(PF<sub>6</sub><sup>-</sup>)<sub>2</sub> were operated in boiling HFE. Even boiling for an hour in that solvent did not cause any substantial change in device brightness and efficiency. In addition to the device results, optical and atomic force microscopy was conducted on a variety of polymeric electronic materials before and after immersion in boiling HFE-7100. No significant change of morphology, nor any cracking or delamination was observed, confirming the orthogonality of HFEs even

under extreme conditions. Figure 1.10 shows a light emitting device lit up in a boiling beaker of the HFE solvent.

Lee and coworkers[79] then synthesized a fluorinated solvent compatible photoresist system, based on a chemically amplified resocinarene molecular glass resist. The resist was used to pattern polymer and small molecule organic semiconductors through both additive and subtractive methods.

Multilayer patterning was also accomplished using this method (as is shown in Figure 1.11), through successive liftoff steps of polyfluorene and ionic complex  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ . Resist was also used to create micro patterned high voltage solar battery which consisted of an array of 300 solar cells in series, with a period of 50  $\mu$  and yield open circuit voltage of 90 V[80]. A polymeric, non-chemically amplified resist was subsequently made by Taylor and coworkers[81] and used to pattern PEDOT:PSS for small-channel OTFTs.

The advantage of this approach is its general applicability to a wide range of materials. It is unusual for a patterning method to be used with both small molecules and polymers equally (not to mention inorganic materials such as metals), and this fact opens up many possibilities of hybrid devices.



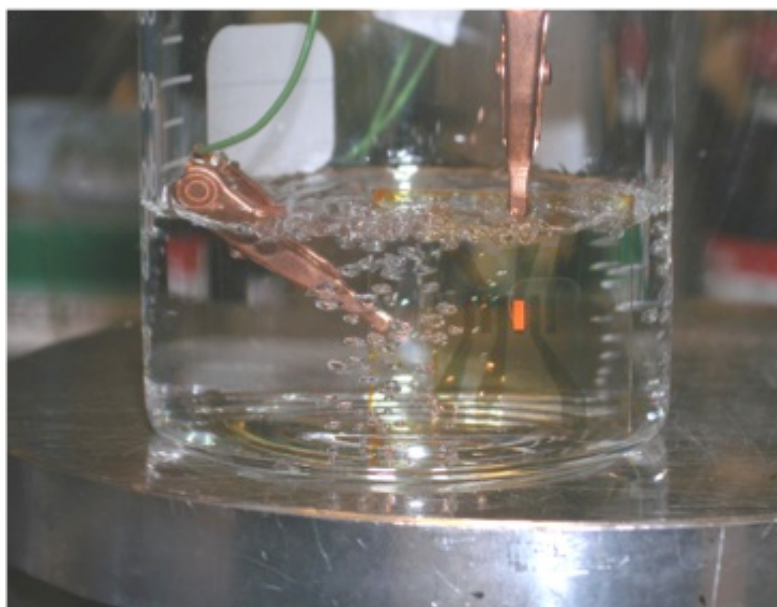


Figure 1.10.  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  device operating in a beaker of boiling HFE solvent.

### ***1.3 Conclusions and General Considerations***

Continued improvement in the technology has moved organic electronics closer to a commercial reality. The techniques that will play a role in helping make that happen depends on many complex technological and market factors. Photolithography has many potential advantages over rival patterning schemes, not the least of which is that it uses manufacturing equipment that already exists at high volumes in established industries such as LCD manufacturing. The potential reduction in startup costs could give organic electronics a way to scale up volumes cheaply and to eventually transition to higher throughput alternatives (to lower costs further) or more flexible alternatives (to enable custom electronics manufacturing) once popular acceptance is achieved. The best opportunities for this kind of scenario is in a market where organic electronic devices are seen as clearly advantageous over other technologies, such as in OLED displays, or flexible electronics based products.

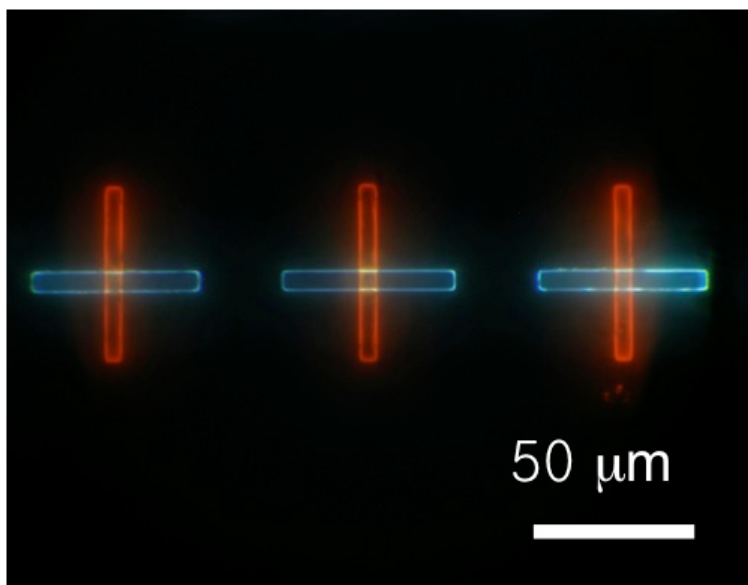


Figure 1.11. Photoluminescence of cross patterns of two different light emitting materials, patterned using calixerene liftoff patterning. The blue line is a polyfluorene and the red is  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ .

Further advancements in organics research may also be aided by these lithographic techniques. Leveraging the high resolutions to explore smaller and smaller material domains and interfaces is a rich avenue of research. It is especially important to use techniques that allow a wide range of materials to be patterned, which is the case in many of the reviewed methods, in order to broaden the scope of study. Indeed the goal of all patterning technologies should be to make the processing of materials the easiest part of device design, putting the emphasis back on materials development, where it began.



## CHAPTER 2

### PARYLENE PATTERNING

#### ***2.1 Introduction***

The initial motivation for wanting to pattern organic electronic materials involved the idea of making waveguides using light-emitting organic materials, in order to create low-cost gain media for light amplification or detection, integrating it into standard photonics structures such as ring resonators, for example. When integrating organic and inorganic materials into a single device, it is very useful if the same manufacturing techniques can be used to pattern each layer and since photolithography is the *sine qua non* of patterning for inorganic materials, efforts were made to make them deployable on the wide variety of soft organic materials as well.

The inspiration for developing the parylene liftoff technique came from one developed by Ilic and Craighead [82]. The technique involved depositing an inert polymer, parylene-C, onto a silicon substrate, etching a pattern into it using photolithography and oxygen plasma RIE, and growing cells in the resulting channels. Once the cells were in place, the parylene could be peeled off of the substrate, leaving patterned cells behind. This process was safe enough to be used with live cells, so it seemed ideally suited to be used with organic semiconducting materials, such as those used to make OLEDs and OTFTs.

This chapter will explain the process in detail, along with the characterization and troubleshooting used to make it workable in a variety of situations. Chapter 3 will deal

with organic transistors made using this process and the characterization of those devices. Chapter 4 will show how the technique was used to make some fundamental measurements of ionic transition-metal complexes and their operation.

### ***2.1.1 Parylene***

Parylene is a chemical vapor deposited (CVD) polymer with a number of useful properties that endow it with applications as a barrier layer in electronic circuits and medical devices [83]. It is deposited near room temperature and gives rise to conformal coatings that can be applied on chemically sensitive materials (such as organics) without damaging them. The coatings are pinhole-free for films of sufficient thickness (typically >500 nm thick). Once deposited, parylene films are nearly inert; they resist solvents, strong acids and bases. As a result, conventional photolithography can be carried out on top of these films. Once developed, the photoresist, serves as a mask for a dry etch step that is used to transfer the pattern to the parylene and the organic film below. In fact, Kymissis et al. have used photolithography to patterned a parylene layer, and selectively etch an underlying pentacene film [84].

In addition, and most importantly, parylene films show relatively weak adhesion to a number of organic films. Their adhesion is good enough for the parylene films to remain securely in place throughout all processing steps indicated in Figure 2.1, including deposition and development of the photo- resist, plasma etching, and handling of the sample. Parylene films can, however, be peeled off from a variety of organic films, a process that can be assisted with adhesive tape. Peeling the parylene

strips off the photoresist in a solvent free manner and leaves the patterned organic material on the substrate.

The structure of the parylene-C dimer and polymer are shown in Figure 2.1 (c). Parylene is synthesized in dimer form from p-xylylene in a several step process. Parylene-C has the addition of a chlorine atom attached to the benzene ring in each monomer.

The chlorine atom makes the resulting film better at blocking moisture penetration and gives it a high resistance to chemical attack. The parylene film is completely linear and highly crystalline following surface polymerization.

### ***2.1.2 Deposition Method***

To deposit parylene, the dimer, which takes the form of fine, white granules, is placed in a furnace that is held under vacuum ( $\sim 1\text{mTorr}$ ). The furnace evaporates the dimer at  $150^\circ\text{C}$ , creating dimeric radicals that are drawn into the next chamber of the system. Inside the second chamber, the gas is heated to  $650^\circ\text{C}$ , where it breaks down into a monomer form and moves towards the main chamber where the substrate is held at room temperature. Parylene spontaneously polymerizes on the surface of the substrate (and the chamber), without going through a liquid stage, which is why the coating is conformal and for the most part uniform, although variations in thickness are observed between the center of the plate and the edges via thin-film interference effects.



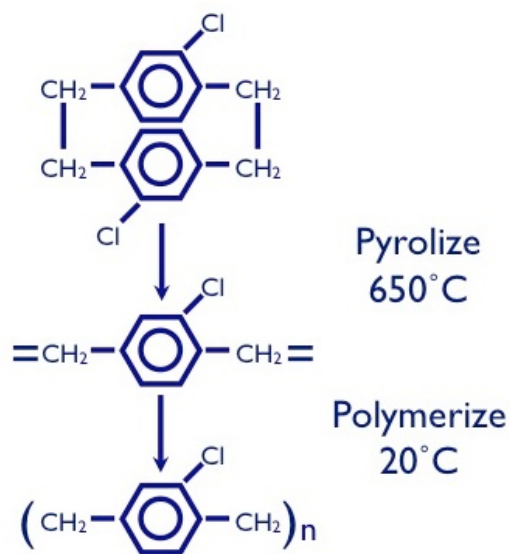


Figure 2.1. The parylene process: (a) Starting with the dimer molecule, the parylene goes through a pyrolysis process to be turned into the monomer form (b), before polymerizing at room temperature on the substrate surface (c).

The parylene deposition for all subsequent experiments took place in a PDS 2010 chamber from Specialty Coating Systems. The deposition thickness is controlled by the amount of dimer used, since the process runs until all of the dimer is used. Typical film thicknesses used were  $\sim 1.5\mu\text{m}$ , from an initial weight of 1.2g of parylene dimer. Thickness was determined using a profilometer on a scratched parylene film that was deposited on a glass slide alongside the wafer.

### ***2.1.3 Properties***

Parylene has a wide range of useful properties that makes it ideal for use with organic electronics. As mentioned before, the deposition process takes place at room temperature. This means that it can be used with materials that cannot withstand high temperatures, as is the case with most organic semiconductors as well as flexible plastic substrates such as polyethylene terephthalate (PET;  $T_m = 260^\circ\text{C}$ ) or polyethylene naphthalate (PEN;  $T_m = 190^\circ\text{C}$ ). It is also a solvent-free deposition process, eliminating potential chemical damage during deposition. These two properties have made parylene attractive as a gate dielectric for top-gated transistor architectures.

The films formed by parylene are conformal (due to the vapor-phase polymerization route) as well as pinhole-free once grown  $\gtrsim 500\text{ nm}$ .

### ***2.1.4 Characterization of parylene etch process***

Parylene etches cleanly in  $\text{O}_2$  Plasma. Etch characteristics were measured on a PlasmaTherm 72 etch tool at CNF using 150 W of power and a pressure of 60 mTorr

(50 SCCM flow rate of O<sub>2</sub>). Shipley 1827 photoresist was used to form patterns on the parylene layer and profile measurements were taken at 1 minute etching intervals, with cleaning of the chamber (using O<sub>2</sub> plasma performed before the test and after 5 minutes of etch time) was performed to keep polymer from building up on the walls of the chamber and then re-depositing on the substrate.

## ***2.2 Subtractive Patterning of Organic Materials***

In photolithography, the film to be patterned is coated with a polymeric photoresist, which is deposited by spin coating. The photoresist is then exposed to light through a photomask, which carries the pattern to be transferred to the film. A developer (typically an alkaline solution) is used to remove the exposed parts in positive photoresists, or the unexposed parts in negative photoresists, replicating the mask pattern (or its reverse) on the photoresist film. Using the remaining photoresist as a contact mask, an etching step is then used to transfer the pattern to the underlying film. The etching can be dry (i.e. reactive ion etching), or wet (i.e. use of suitable solvent), depending on the nature of the film to be etched and the substrate. Finally, the photoresist is stripped off by an appropriate solvent. The incompatibility of organics with conventional lithography arises primarily due to the solvents used for the deposition, the development and the removal of the photoresist. The solvents used in these three steps have, with a few exceptions [85], detrimental effects on organic films, including dissolution, cracking, swelling, and delamination. Although chemical modification of conjugated polymers to include a photoactive element that allows their

direct (without using a photoresist) patterning has been recently demonstrated [86], such a solution requires custom chemistry for each material used.

By adding a parylene interlayer, the harmful effects of the photolithography chemicals are mitigated. In this modified subtractive process (shown in Figure 2.2 (a)), a layer of parylene is deposited on top of the organic after deposition. Once a sufficiently thick coating ( $>500$  nm) has been deposited, the organic material is sealed in a conformal coating. Exposure to solvents and caustics has no effect on the underlying film, as the parylene provides a complete chemical barrier. Since the parylene also tends to wrap around the edge of the film to coat the backside of the wafer as well, the film stays intact through immersion and no chemicals can enter from the side either. A standard lithographic process is done on top of the parylene layer, with resist left in places where organic semiconductor film should remain after processing. With a positive tone resist system (as was used here), which means that light exposure takes place in the regions designated for removal. Once the resist has been developed, the pattern is transferred through the parylene layer to the organic layer beneath. Since nearly all organic semiconductors are etched with the same oxygen plasma used to etch parylene, only a single etch process is needed.

The photolithography steps were performed on a GCA Autostep 200 as well as an HTG contact aligner. The primary photoresist used was Shipley SPR 220 3.0, spun between 3000 and 4000 rpm, yielding films of  $2.5\text{--}3.2\mu\text{m}$  as measured by a FilMetrics optical thickness monitor. The chemistry of SPR 220 is similar to that of other i-line (365 nm) photoresists in that it is a DNQ Novalac resist. The novalac resin provides

the structure and is generally base soluble unless mixed with the DNQ solubility inhibitor. Once exposed to light, the diazonaphthoquinone (DNQ) undergoes a Wolff rearrangement to form a ketene, after which it no longer inhibits the solubility of the novalac resin.

### ***2.3 Additive Patterning of Organic Materials***

A second popular way for patterning films using photolithography involves lift-off. In the lift-off process, the photoresist is used as a stencil mask. It is deposited directly on the substrate, and it is exposed and developed to leave parts of the substrate bare. The film to be patterned is subsequently deposited and coats the bare parts of the substrate and the surface of the photoresist. An appropriate solvent is used to dissolve the remaining photoresist, removing the part of the film that was deposited on it. The problem with this process arises due to the incompatibility of organics with the solvent used for the removal of the photoresist.

Figure 2.2 (b) shows an approach for carrying out the above photolithographic process on organic films. Parylene is used here in the place of the photoresist to enable the dry lift-off of the organic. This approach, which relies on the limited adhesion of parylene to the substrate, was originally developed by Ilic and Craighead for patterning of biological materials such as proteins and cells [82]. The actual peeling process used a combination of Scotch tape and tweezers to peel the entire film from the substrate, starting from an edge. Once the edge is lifted, the film separates easily. The force required to peel parylene from various substrates has been investigated by Takeuchi et al. [87].

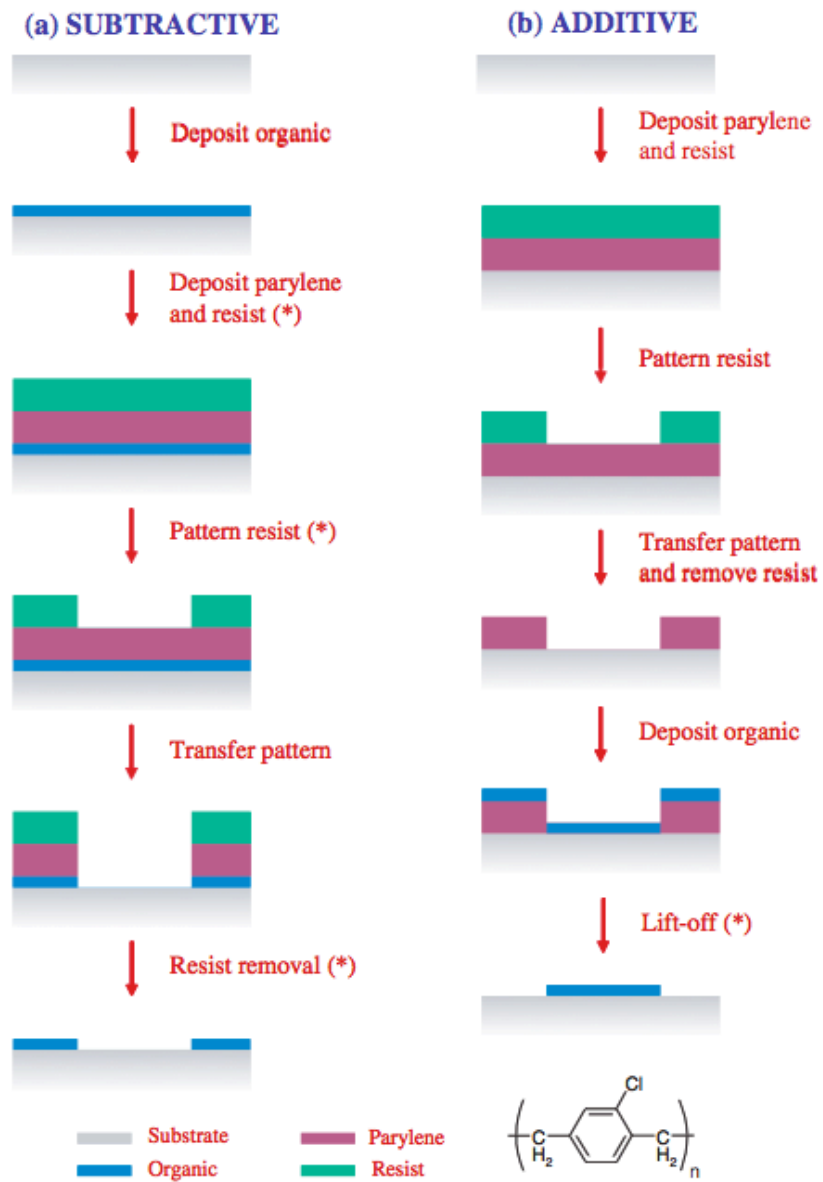


Figure 2.2. (a) Subtractive parylene patterning process. (b) Additive or liftoff parylene patterning process.

Examples of organic films patterned using this approach are shown in Figure 2.3. These films are the direct image of the photomask when positive tone photoresist is used, and the overall process is additive. Figure 2.3 (c) shows 1  $\mu\text{m}$  wide lines of PEDOT:PSS on a 10  $\mu\text{m}$  pitch, and Fig. 2.3(d) shows spiral lines with a 4  $\mu\text{m}$  width made from ruthenium tris-bipyridine,  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ , a material used in OLEDs [18]. Finally, Figure 2.3 (a) shows an array of square pixels with a 4  $\mu\text{m}$  edge made from pentacene, an organic semiconductor used in OTFTs [88]. Such structures can be used, for example, to define pixels in OLED displays, or to define the p- and n-type regions in TFT circuits. An AFM micrograph shown in Figure 1.9(b) reveals well-defined edges and uniform pentacene thickness.

The structures in Figure 1.9 (from Chapter 1) were fabricated as follows: Parylene was deposited on oxidized silicon wafers as described previously. Its patterning was also conducted in the same way as in the subtractive approach, but the photoresist was hard baked prior to exposure (it was found that heating at temperatures as high as 130° C did not appear to affect the integrity of the parylene layer). After the parylene patterning, the residual photoresist was stripped off with an acetone/isopropanol bath before the deposition of the organic film and the wafer was treated in a UV/ozone cleaner. The organic material was subsequently deposited by spin coating (PEDOT:PSS and  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ ), or vacuum sublimation (pentacene). The parylene layer was peeled off mechanically, as in the subtractive approach.

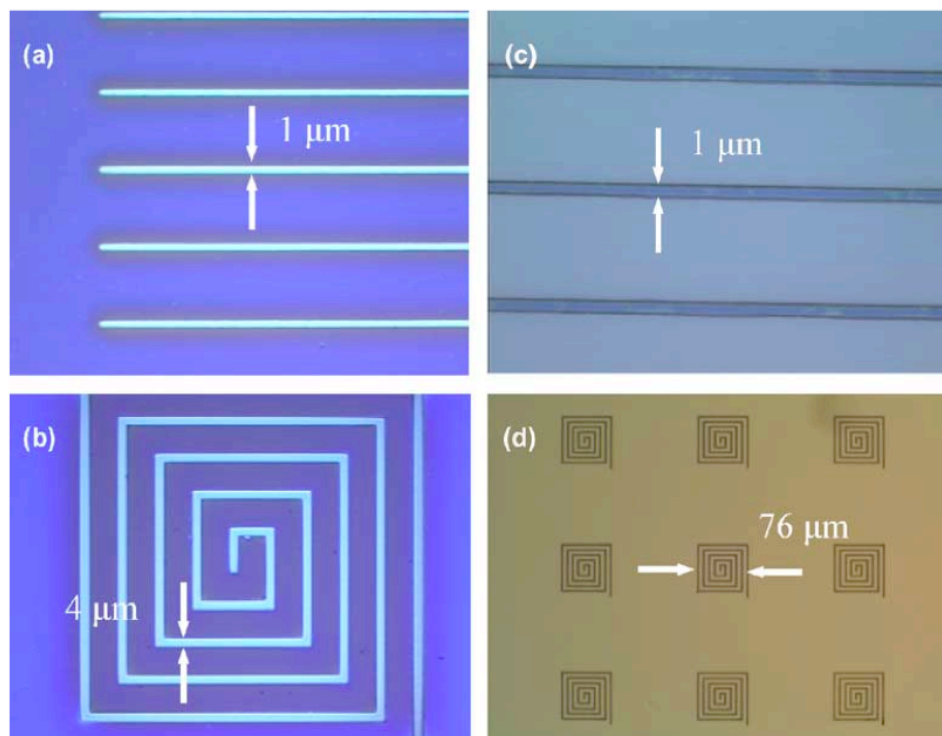


Figure 2.3. (a) and (b) show trenches etched in PEDOT:PSS using the subtractive parylene patterning technique. (c) PEDOT:PSS and (d)  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  patterned with the additive technique.



## ***2.4 Film Adhesion***

The prior examples were all processed on silicon wafers. Glass was also commonly used in this experiment and give a similar surface to silicon, because bare silicon grows a native oxide layer upon exposure to air. This layer is usually  $<2$  nm, but is sufficient to give the surface a glass-like, hydrophilic surface. The adhesion between the substrate surface and the parylene is of utmost importance, because it needs to be strong enough to not peel off during processing (e.g. bubbles forming through pinholes or delamination during resist development), but not so strong that it doesn't yield to mechanical pressure during the peeling process.

Peeling the films from pentacene seemed to be difficult after etching. In such cases the pentacene films tended to come up with the parylene layer, leaving a nearly clean substrate surface. We speculated that a couple of factors are contributing to this result. First, pentacene is generally hydrophobic and has a Van Der Waals attraction between molecules through the lining up of the aromatic rings. A similar interaction can happen between the pentacene and the parylene. The aromatic rings in the parylene molecule will have a strong interaction with the pentacene molecules and this will cause them to stick. Combined with the generally weak interaction of pentacene with the substrate surface (one of the goals of growing large-grained pentacene crystals on the wafer is to make the pentacene crystals "stand up", by treating the surface with a SAM layer), the film tends to fully delaminate upon peeling. Second, pentacene can form very rough films due to their three-dimensional growth[89]. This

roughness increases the surface area of interaction between the pentacene and the parylene, enhancing the adhesion effect.

As an indicator of the potential viability of this technique, subtractive parylene patterning of organic semiconductors seems like it will be a difficult prospect. Most high-performing organic semiconductors have structures very much like pentacene, with multiple aromatic rings and at least some surface roughness. It is perhaps possible to leave the parylene layer on top as a kind of encapsulation layer (as Kymissis has done), but it limits the potential architectures employed by the manufacturers.

In certain cases, as in the example of gold, parylene sticks too strongly, but certain measures can be used to get around the problem. Chapter 4 discusses this case in more detail.

## ***2.5 Film Contamination***

Another problem encountered during the optimization of this process is the problem of particulate contamination in the parylene film. Scanning electron microscopy (SEM) images of etched gold films revealed spikey features covering the surface of the trenches, where there should have been smooth films (the gold was etched with an anisotropic ion milling process). Figure 2.4 shows the spikes under SEM.

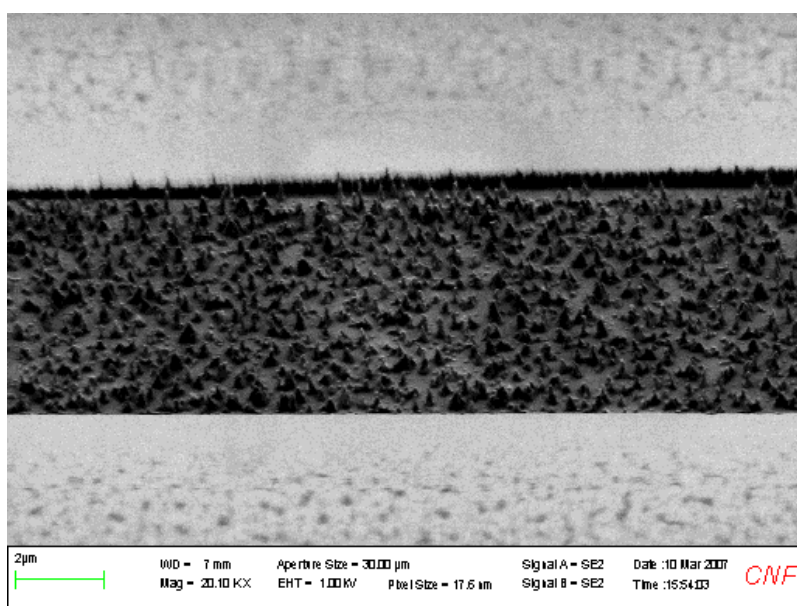


Figure 2.4. SEM image showing spike formation in the trench between two gold electrodes. Image is taken after coating with  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ .

The problem seemed to be coming from large numbers of particles acting as an etch mask to the ion milling, creating the conical spikes. We suspected contamination and found that the parylene film contained trace amounts of aluminum. The source of the aluminum contamination was eventually traced back to the Brillo pads used to scrub the parylene off of the cold trap. They are made of spongy aluminum oxide and create a fine dust during the abrasion process.

## ***2.6 Conclusion***

A method for patterning a variety of organic electronic materials was presented using the inert polymer parylene. Two common methods of photolithographic patterning, etching and liftoff, can be achieved using parylene as an intermediary, to assure that the chemicals associated with the process are not introduced into the organic system.

The subtractive method was successfully shown to pattern hydrophilic materials such as PEDOT:PSS, but for more common organic semiconductors, the parylene could not be peeled away from the top of the OSC films without delaminating them. Although it may be useful to leave the parylene layer on top in many circumstances as an encapsulation layer, this fact limits its usefulness.

The additive method represents a novel way to pattern organic materials and is much more robust in the variety of materials that can be patterned in this way. However the peeling process itself can be limited by the fact that isolated pieces of film are difficult to remove in the way described here, because they don't connect to the larger film and come up continuously. This is not necessarily a showstopper as

commercially available delaminators might be used to make this work, but such a process was not investigated here and shall be left for future investigators.



## CHAPTER 3

### ORGANIC THIN-FILM TRANSISTORS MADE WITH PARYLENE PATTERNING

#### ***3.1 Introduction to Organic Thin-Film Transistors***

The techniques developed in Chapter 2 can find application in many areas. Here we demonstrate that the subtractive and additive parylene patterning methods can be used to pattern elements of an organic thin-film transistor. First, it is demonstrated that narrow-channel devices using the conducting polymer polyethylene dioxythiophene:polystyrene sulfonate (PEDOT:PSS) as the source and drain electrodes. These devices are fabricated using the parylene liftoff technique covered in the previous chapter and yields channel lengths far exceeding those possible with competing techniques such as inkjet printing. After that, devices that have both the channels and active material (pentacene in this case) patterned through a combination of parylene techniques are presented.

##### **3.1.1 Device Operation**

Organic thin-film transistors (OTFTs) are a subset of thin-film transistors that use carbon-containing materials as the active semiconductor. An OTFT is a three terminal solid state device whereby current driven between two electrodes, the source and drain, is modulated through the application of an electric field, which controls the accumulation of charge carriers in the semiconducting region between the source and drain, the channel. Figure 3.1 illustrates a typical device architecture.

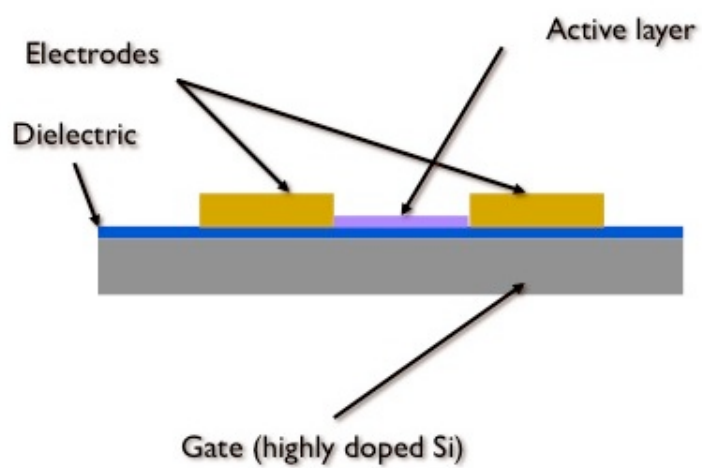


Figure 3.1. Typical OTFT device architecture.



The fact that OTFTs use organic molecules or polymers as channel materials rather than crystalline semiconductor materials such as silicon or gallium arsenide changes the details of charge transport across the channel region. Nevertheless, we typically use a thin-film transistor model to describe their behavior, as it is similar enough for large devices (one or several microns) to be useful. The major difference between crystalline inorganic semiconductors and organic materials is that the former has delocalized charge carriers that occupy valence and conduction bands, reflecting the long-range order of the materials and the relatively strong bonding between atoms. Organic materials, by contrast, are often bound by Van der Waals forces, and electron and hole transport (most often hole transport dominates in organic materials) happens through a hopping motion. The consequence of this is that charge-carrier mobilities for these materials is often quite low ( $0.01\text{--}2.0\text{ cm}^2/\text{V}\cdot\text{s}$ ) compared to silicon ( $\sim 1000\text{ cm}^2/\text{V}\cdot\text{s}$ ). Polycrystal silicon ( $\sim 10\text{ cm}^2/\text{V}\cdot\text{s}$ ) and amorphous silicon ( $\sim 0.5\text{ cm}^2/\text{V}\cdot\text{s}$ ) are more comparable to the performance levels of organic transistors and are useful in the same place: as large area thin-film devices for applications such as display backplanes.

The equivalent to the valence and conduction bands for organic materials are the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), respectively. The HOMO and LUMO levels are created by  $\pi$ -bonded molecular orbitals that cause an energy splitting at carbon-carbon double bonds.

When in operation, charge carriers are induced by the gate electrode into the channel. If we use the gradual channel approximation from MOSFET devices, the (hole) current is:

$$I_{sd} = \mu \frac{W}{L} \int_0^{V_{sd}} Q(V) dV \quad (3.1)$$

where  $\mu$  is the field-effect mobility (in  $\text{cm}^2/\text{V}\cdot\text{s}$ ),  $L$  is the channel length (distance from source to drain),  $W$  is the width of the channel,  $V$  is the potential at the surface of the organic semiconductor and  $Q(V)$  is the charge per unit gate area as a function of surface potential.

We can further use the approximation that the holes induced by the field from the gate electrode form a thin sheet of charge,

$$Q(V) = -C_{ox}(V_g - V_T - V) \quad (3.2)$$

where  $C_{ox}$  is the capacitance of the gate across the gate dielectric and  $V_T$  is the voltage threshold (the onset of gate-induced current). We can now substitute this into equation (3.1) to get,

$$I_{sd} = -C_{ox} \mu \frac{W}{L} \left[ (V_g - V_T) V_{sd} - \frac{1}{2} V_{sd}^2 \right] \quad (3.3)$$

In the so-called linear regime,  $V_{sd}$  is small, so we can neglect the squared term, leaving,

$$I_{sd} = -C_{ox}\mu\frac{W}{L}(V_g - V_T)V_{sd} \quad (3.4)$$

Once  $V_{sd}$  reaches the effective gate voltage ( $V_g - V_T$ ), the device enters saturation mode as the accumulation channel ends near the drain electrode. The current is then,

$$I_{sd} = -C_{ox}\mu\frac{W}{L}(V_g - V_T)^2 \quad (3.5)$$

### 3.1.2 Performance Parameters

From equations (3.4) and (3.5) we can see the relevant parameters to achieving high performance from an organic transistor. Mobility is certainly a key factor in getting a high output current, but gains can also be made by improving the gate capacitance (e.g. by increasing the dielectric constant or making a thinner gate dielectric material) or changing the channel geometry. It is this last area that patterning can help improve device performance.

Typically, the channel width of a device is constrained somewhat by the total device area or other factors (such as fill factor in a display backplane). Shrinking the channel length, then is the most promising path towards achieving higher performance, given a certain organic semiconductor ( $\mu$  is fixed) and dielectric material ( $C_{ox}$  is fixed). Given the limitations of inkjet printed channels are around  $10\mu\text{m}$  without additional photopatterning of dewetting layers, photolithographically defined channels can bring a performance boost of nearly an order of magnitude.

### 3.1.3 Patterning Requirements

In a fully realized transistor connected to a larger circuit, patterning is used to define every layer in the OTFT. Gate layers must be patterned in order to control the current of each individual transistor separately. The dielectric layer must be patterned not only to allow outside electrical contacts, but also to connect the gate of one transistor with the source or drain or another transistor. The holes through which such connections are made are known as vias.

Even transistors that are designed to measure individual device performance, through they may dispense with gate and dielectric patterning (often using a highly doped silicon wafer for the gate and thermally grown oxide as the gate dielectric), need some form of patterning to define the active region and the source/drain electrodes. It is not strictly-speaking necessary to pattern the organic layer on such test devices, but off current is often too high in unpatterned devices, due to multiple charge carrier pathways, negatively affecting the on/off ratio. Patterning the source/drain electrodes defines the channel dimensions, which plays a crucial role in determining the saturation current and switching speed in circuits.

A number of techniques used to pattern both the active layer and source/drain layer were discussed in the first chapter. In the case of bottom contact transistors, either metal or conducting polymer electrodes have been used to make working OTFTs. Metal electrodes are most often patterned using photolithography, since in this architecture, the organic material is not deposited until after source/drain patterning has taken place. For conducting polymer electrodes, usually polyethylene

dioxythiophene:polystyrene sulfonate (PEDOT:PSS), inkjet printing is often the preferred method since photolithography cannot be directly used with this material. It is also important to compare these devices with one made using a shadow mask to pattern source and drain electrodes on top of the active layer. Although shadow masking (in which metal atoms are evaporated through a perforated metal film) can form transistors with high intrinsic performance (because the active layer is deposited first, onto a relatively uniform substrate), it is severely limited in resolution to around 10–20  $\mu\text{m}$ .

### ***3.2 Peeled Electrode Devices***

#### **3.2.1 Motivation**

The first experiment was to use the liftoff parylene patterning technique to pattern PEDOT:PSS electrodes for bottom contact pentacene transistors. The geometry of these devices will be bottom contact with unpatterned gate and an active layer consisting of blanket deposited pentacene. The smallest channel lengths attempted in this experiment were 2  $\mu\text{m}$ .

As was detailed above, the goal of this experiment is to see whether electrodes patterned with the parylene liftoff technique would have performance improvements compared with lower resolution techniques, such as shadow mask patterning.

#### **3.2.2 Experimental**

A highly doped silicon wafer ( $\rho < 0.005 \Omega\text{-cm}$ ) was purchased from Silicon Quest and was oxidized in the furnace at 1000–1100°C for 60–90 minutes to form a 300nm  $\text{SiO}_2$  layer. Oxide thickness was determined with a FilMetrics film analysis tool. On top of

the oxide layer, 1.5 $\mu$ m of parylene was deposited, as measured with profilometry on a glass slide in the chamber with the wafer. Shipley SPR 220 3.0 photoresist was spun at 4000rpm to obtain a 2.5 $\mu$ m film. The film was post-apply baked (PAB) at 130°C for 90 seconds. The film was exposed on the GCA Autostep 200 DSW i-line Wafer Stepper for 0.13 seconds using a dark field mask to obtain the source/drain patterns. The film was post exposure baked (PEB) for 90 seconds at 130°C. After developing the resist in MIF 300 (TMAH based developer) for 60 seconds, the patterns became clear at the bottom, indicating the removal of most of the resist in the exposed area. Usually some residue is left, but the subsequent etch step eliminates this material.

The wafer was etched in an oxygen plasma reactive ion etch chamber (PlasmaTherm 72), for 13–15 minutes, until the parylene is completely removed from the trenches. Residual resist is stripped with acetone/isopropanol on the spin coater. The wafer then has a layer of patterned parylene on top of silicon oxide. PEDOT:PSS (Baytron-P) was spin coated onto the wafer at 3000rpm from a water suspension. The film was briefly heated on a hot plate ( $\sim$ 120°C) to drive off most of the water from the film. When the film changed from a “wet” appearance to a “dry” appearance, the parylene film was peeled from the wafer mechanically, using scotch tape or tweezers to grip the edge of the film. The poor adhesion between the parylene and the substrate allowed for facile peeling and unless the parylene film was thinned significantly through heavy over-etching, the film would peel from the four-inch wafer in one piece. The patterned PEDOT:PSS films were baked at 120°C for 1–2 hours under

vacuum, in order to drive out any remaining water, which may affect pentacene performance. The wafer was then cleaved into individual dies.

Pentacene (used as received with no further purification) was deposited onto the substrate at a rate of  $0.1\text{\AA}/\text{s}$  at a pressure of  $< 1 \times 10^{-6}\text{Torr}$ . After deposition, the backs of the wafers were scratched with a diamond scribe to remove the thermally grown oxide layer and silver paste was painted on in order to allow for electrical contact to the silicon.

Devices were tested in a vacuum probe station, using Keithley source meters controlled by a computer running Labview.

### **3.2.3 Results**

An image of the patterned electrodes can be seen in Figure 3.2(a). The channel length of this device is  $2\mu\text{m}$  and the width is  $20\mu\text{m}$ , giving a W/L of 10. Figure 3.2(b) shows the current-voltage (IV) characteristics for the device. The measured mobility was  $7 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$ . Top performing pentacene transistors can achieve mobilities of  $\sim 1 \text{ cm}^2/\text{V}\cdot\text{s}$ , so this device is performing below par.

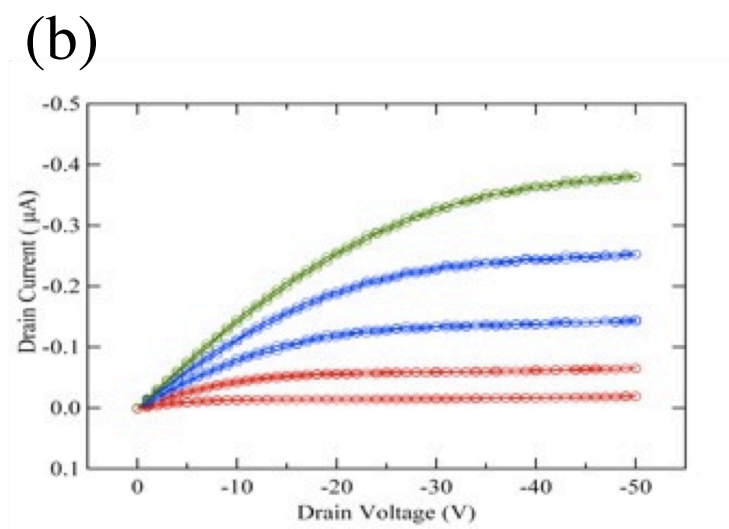
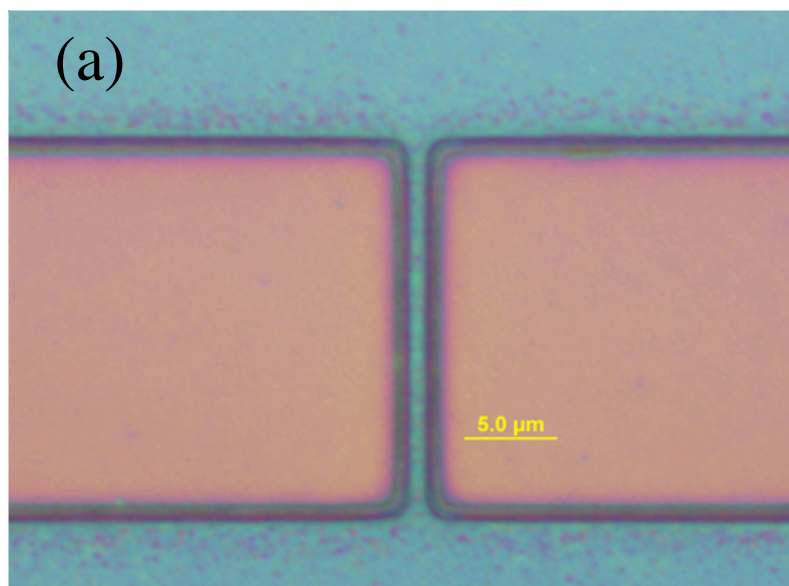


Figure 3.2. (a) Device made using the peeled electrode parylene technique. (b) IV characteristics for the 2 $\mu\text{m}$  channel device with pentacene electrodes.



### 3.2.4 Discussion

The peeling process worked well for these devices and on most wafers, the entire film could be removed in a single piece. The technique was reproducible down to the feature sizes sought, which were  $2\mu\text{m}$  in this case. In all cases, the peeling direction was along the width of the channel so that the thin strip of parylene would be intact during peeling. This part may be the ultimate limit to the size of the channel length using this technique.

The performance of the devices was disappointing. It should be noted that devices made in our lab at the time were not reaching  $1\text{ cm}^2/\text{V}\cdot\text{s}$ , but were on the order of  $0.1\text{ cm}^2/\text{V}\cdot\text{s}$ , so the drop was a little bit more than one order of magnitude, compared to our capabilities (slow dep. rate, shadow mask patterned top contacts). Our devices improved when we found a better supplier for the pentacene (to achieve the best results, other labs would zone refine their materials before use) and started using a dedicated deposition chamber that was not also used for n-type materials. It is also typical to use self-assembled monolayers to enhance the long range order and, as a result, the mobility of the pentacene layer. Such treatment was not done in this case, although there is no reason why it couldn't be done here.

The best explanation for the decrease in performance comes from looking at both the image and the IV data. There is a bit of additional contact resistance above the norm in this device, and looking at the image, the reason can be seen. One side-effect of the parylene liftoff process for patterning spin-coated films is that it tends to form a lip at the edge. It is very difficult to get a completely flat film all the way out to the

edge of the feature because of the adhesion of the spun on material, PEDOT in this case, to the sides of the parylene. Since the parylene film is  $\sim 1.5 \mu\text{m}$  high and the typical PEDOT film is 100 nm thick, there is a significant discontinuity with the feature. From the image, the PEDOT film looks significantly darker near the edge of the feature than in the middle. When pentacene is deposited on top of the structure, a discontinuity forms and the grains will be particularly small at the boundary, reducing the mobility across the channel.

It is not known whether this problem can be fixed or not, using this particular technique. A subtractive approach can be used to pattern the PEDOT layer, which is what we did next.

### ***3.3 Inset Devices***

#### **3.3.1 Motivation**

The last experiment suffered from poor performance, primarily because of the non-uniformity of the liftoff patterning at the edge of the electrodes. Here, a different method is employed to try to solve the problem, while at the same time, patterning the active layer.

#### **3.3.2 Experimental**

Similar wafer preparation was used as in the last experiment. The transistor was fabricated by first applying the additive approach to pattern 1 mm long,  $50 \mu\text{m}$  wide stripes of PEDOT:PSS. A second additive step was then used to deposit a  $2 \times 75 \mu\text{m}^2$  island of pentacene, which was done by vacuum sublimation. The etching step that

preceded the deposition of the pentacene partitioned the PEDOT:PSS stripe in the middle, defining the source and drain electrodes, separated by a 2  $\mu\text{m}$ -long channel.

### **3.3.3 Results**

As can be seen in Figure 3.3(a), the pentacene is contained in a well-defined channel going across the PEDOT stripe, with none of the raised-lip problems of the previous devices.

Two micrometer channels were easily made using this technique, as there is no limiting factor that the stripe defining the channel needs to survive the liftoff process. Here, only a groove interrupts the intact parylene films, so peeling in any direction is feasible.

Figure 3.3(b) shows the resulting device performance. The mobility from this device was  $3 \times 10^{-2} \text{ cm}^2/\text{V}\cdot\text{s}$ . Some charge injection limiting can be seen from the slight upward curve in the linear regime.

### **3.3.4 Discussion**

The improved performance may be due to the elimination of the electrode lip, and the general improvement in long-range order that this causes. The contact limitation seems to come from the limited interface between the pentacene and the polymer electrode. In typical OTFT devices, even with patterned OSC materials, there is typically an overlap of several microns between the electrode top and the active material. This allows injection over a larger area and reduces the chance of having a bottleneck at the contact limiting the current through the device.

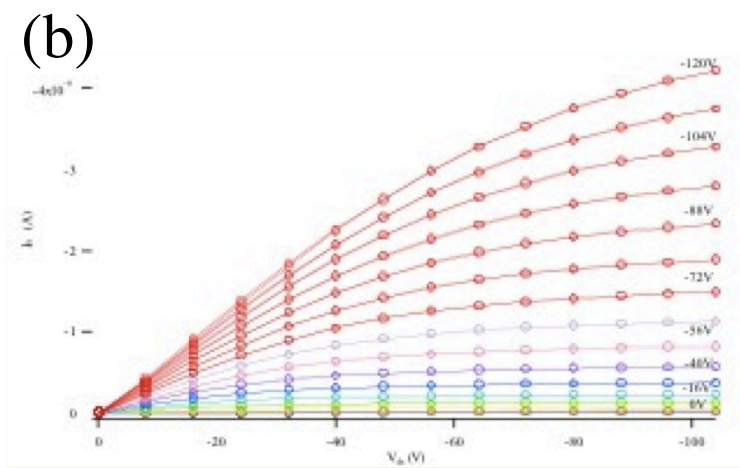
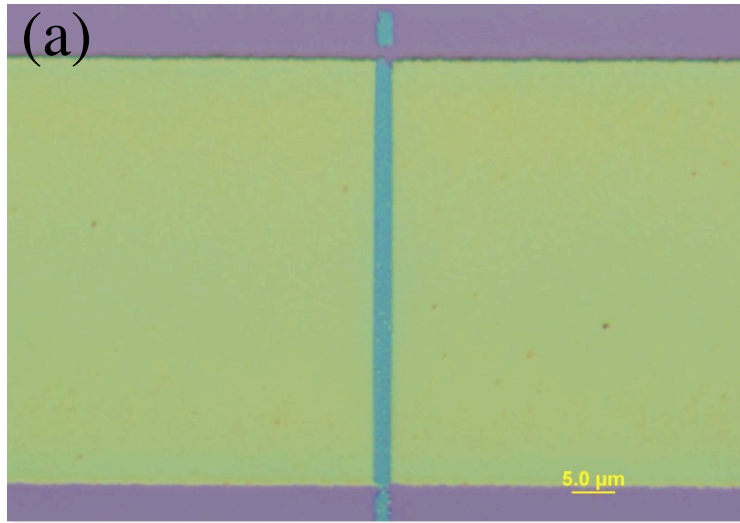


Figure 3.3. (a) Completed inset device. (b) IV curve of device.

An improved device might have etched electrodes, without using the same parylene groove to pattern the pentacene, allowing for a greater overlap. When polymer electrodes are used, however, further patterning steps that lay across the electrode will always etch the electrode when the parylene is being etched, so such a scheme would be limited to a unpatterned pentacene layer. Considering the lack of overlap, the device performance is remarkable, and further studies may make even more breakthroughs in performance.

### ***3.4 Conclusion***

We have demonstrated the usefulness of both the additive and subtractive parylene patterning technique in making organic thin-film transistors. Although the present devices are not pushing the state-of-the-art in terms of performance, they demonstrate the concepts well, and the potential for novel devices to be made using this technique.



## CHAPTER 4

### DIRECT MEASUREMENT OF THE ELECTRIC-FIELD DISTRIBUTION IN AN IONIC TRANSITION-METAL COMPLEX

#### ***4.1 Introduction to iTMCs***

Ionic transition-metal complexes (iTMCs) are very similar to OLED devices in that they are organic small molecules that emit light when biased between two electrodes. The fundamental difference between the two types of devices is that iTMCs contain mobile ions that play a role in charge injection and transport. The main advantage of iTMC devices is that the electrode work function plays a far less important role than it does in traditional OLEDs; that is that high work function electrodes can be used for both the anode and cathode. This is important because one of the primary decay mechanisms in OLEDs is degradation of the low work function cathode due to atmospheric oxidation.

##### **4.1.1 Comparison with OLEDs**

In an OLED device, a light emitting material is sandwiched between two electrodes, designated the anode and the cathode, with one or several intermediate layers designed to facilitate charge injection or transport. In order to enable efficient operation, the anode work function must lie very close to the energy level of the HOMO of the OLED material and the cathode must have a work function near the material's LUMO.

##### **4.1.2 Ionic Transition Metal Complexes**

Ruthenium tris-bypyridine ( $\text{Ru}(\text{bpy})_3$ ) is a prime example of a transition metal complex iTMC material. The chemical structure, shown in Figure 4.1, where it can be seen that

the complex carries a net charge of +2 that is offset by two hexafluorophosphate ( $\text{PF}_6^-$ ) counter ions.

## ***4.2 Kelvin Probe Measurement of Ru(bpy) Planar Device***

### ***4.2.1 Motivation***

The field of solid-state ionics encompasses a broad range of materials, such as ceramics, polymers and glasses[90, 91]. The identifying characteristic of this class of materials is their ability to transport ions in the solid state. Ionic space-charge effects can be exploited to facilitate changes in the optical, mechanical or electrical properties, giving rise to a host of applications in chemical sensors[92, 93], electrochromic windows[94], fuel cells[95], batteries[96, 97] and solar cells[98, 99]. Of particular interest within this class of materials are mixed conductors, in which, in addition to ionic conductivity, significant electronic conductivity is also present. The coupling between ionic and electronic carriers in mixed conductors offers rich physics and unique potential in devices[90].

An example of such a device is the light-emitting electrochemical cell (iTMC), which recently received attention for its potential in flat-panel display and solid-state lighting applications[99–133]. iTMCs consist of a mixed-conductor layer sandwiched between two metal electrodes. A typical example of a mixed conductor used in iTMCs is ionic transition- metal complexes (iTMCs), such as ruthenium tris-bipyridine hexafluorophosphate[99,118–133],  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ .



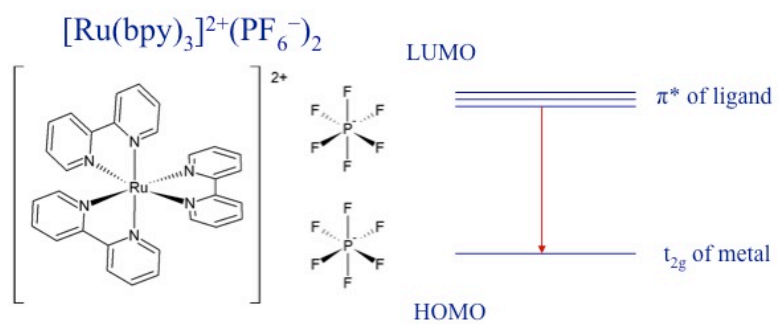


Figure 4.1.  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  diagram and energy levels of HOMO and LUMO.

An example of such a device is the light-emitting electrochemical cell (iTEC), which recently received attention for its potential in flat-panel display and solid-state lighting applications[99–133]. iTECs consist of a mixed-conductor layer sandwiched between two metal electrodes. A typical example of a mixed conductor used in iTECs is ionic transition- metal complexes (iTECs), such as ruthenium tris-bipyridine hexafluorophosphate[99,118–133],  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$ . The ruthenium complex is an (intrinsic) molecular semiconductor, in which the highest occupied molecular orbital (HOMO) is the  $t_{2g}$  of the metal, and the lowest unoccupied molecular orbital (LUMO) is a  $\pi^*$  orbital of the ligands. On the application of a bias in this iTEC, holes and electrons are injected from the anode and the cathode, respectively, into the ruthenium complex. These carriers are transported towards the opposite electrode via hopping, and may recombine to produce light emission with a characteristic colour that corresponds to the energy gap of the complex. Critical to the operation of these iTECs are the counter ions ( $\text{PF}_6^-$  in this example), which are mobile in the film and at room temperature. Their redistribution on the application of a bias assists the injection of electronic carriers and enables novel device architectures[99,127,128,130,132], including fault-tolerant large-area illumination panels[128,130] as well as illumination panels that can be plugged directly into an a.c. power outlet[130].

The presence of both ionic and electronic carriers in iTECs, as well as other mixed conductors, poses a significant challenge in understanding their device physics. This is illustrated by the lack of consensus on the distribution of the electric field in iTECs[99–133]. The two extremes are represented by the electrochemical model

[100], which predicts a high electric field in the bulk of the film, and the electrodynamic model[104], which predicts high electric fields near the electrodes. In addition to its significant fundamental interest, understanding the device physics of mixed conductors is essential to enable the engineering of better devices. The two models are shown in Figure 4.2, on the right.

Electric force microscopy (EFM) enables direct microscopic determination of local potential. The voltage applied to a metal-coated cantilever is swept, producing a frequency shift that is parabolic about the local potential[134,135]. Unfortunately, the sandwich-type configuration that is used in iTMCs to minimize the thickness of the iTMC layer is not amenable to facile probing.

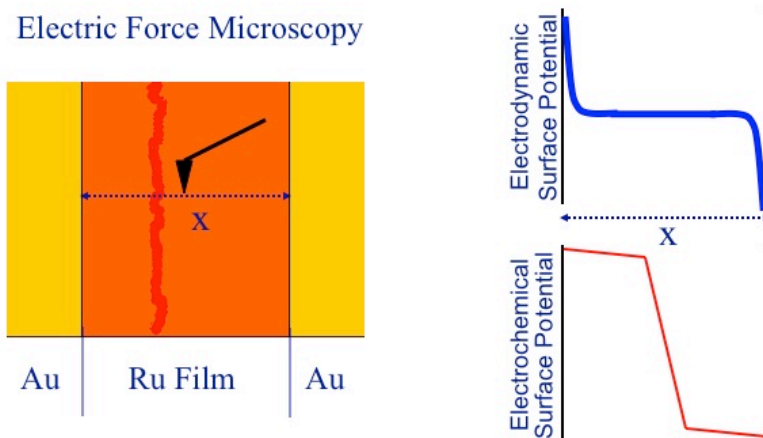


Figure 4.2. Diagram of EFM experiment and comparison of two models.

To enable a direct measurement of the electric-field distribution in iTMCs with EFM, planar devices were fabricated in which a  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  film was spin-coated onto an insulating substrate with pre-patterned Au electrodes (illustrated in Figure 4.2).

#### 4.2.2 Kelvin Probe Microscopy

Frequency-shift electric force microscopy in high vacuum ( $10^{-5}$  torr) was used to probe local electric potential and capacitance[134]. We used a commercial cantilever (MikroMasch NSC18/Ti-Pt) with a spring constant,  $k_0$ , of 3.5 N/m , a resonance frequency,  $f_0$  , of 75 kHz, and a vacuum quality factor,  $Q$ , of  $1 \times 10^4$ . In these experiments, the cantilever was retracted to a height,  $z$ , of 200 nm above the sample surface. This lift height determines the spatial resolution, which was approximately 200 nm in the experiments reported here. The dependence of cantilever frequency,  $f$  , on tip voltage,  $V_t$ , can be approximated by

$$f(V_t) \approx f_0 - \frac{f_0}{2k_0} \frac{\partial^2 C_{ts}}{\partial z^2} (V_t - \Delta\phi)^2 \quad (4.1)$$

where  $C_{ts}$  is the tip-sample capacitance,  $V_t$  is the tip potential and  $\Delta\phi$  is the contact potential difference between the tip and sample. The cantilever is scanned back and forth between the source and drain electrodes along a line, and at each position in the gap the cantilever frequency is measured as a function of the tip-gate voltage. At each location in the line scan, the resulting frequency-versus-voltage curve is fitted to the

above equation. The resulting uncertainty in the electrostatic potential,  $\Delta\phi$ , is approximately 30 mV.

#### **4.2.3 Measurements of Unpatterned Devices**

Figure 4.3 shows the distribution of the potential (Figure 4.3(a)) and the electric field (Figure 4.3(b)) in these devices. The thick green trace, which indicates the first measurement after the application of a 5 V bias, shows that the potential drops linearly as a function of distance between the two electrodes. The corresponding electric field is approximately constant, indicating that the  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  film acts as a resistor. After 1 h of continuous application of bias, during which steady-state is reached, the electric field (thick red trace) shows a small enhancement near the cathode, accompanied by a slight decrease throughout the rest of the  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  film.

#### **4.2.4 Discussion**

On the basis of this electric-field distribution, it is not possible to unambiguously discriminate between the two models of iTMC operation, and hence it is not possible to determine the underlying device physics.

A closer observation of the data, however, reveals considerable changes of the potential over the metal electrodes. This can be seen in Figure 4.3 (c), where the potential over the anode decreases substantially with time. This phenomenon can be understood by the diffusion of the  $\text{PF}_6^-$  counter ions over the metal electrode. A schematic illustration is shown in Figure 4.4.

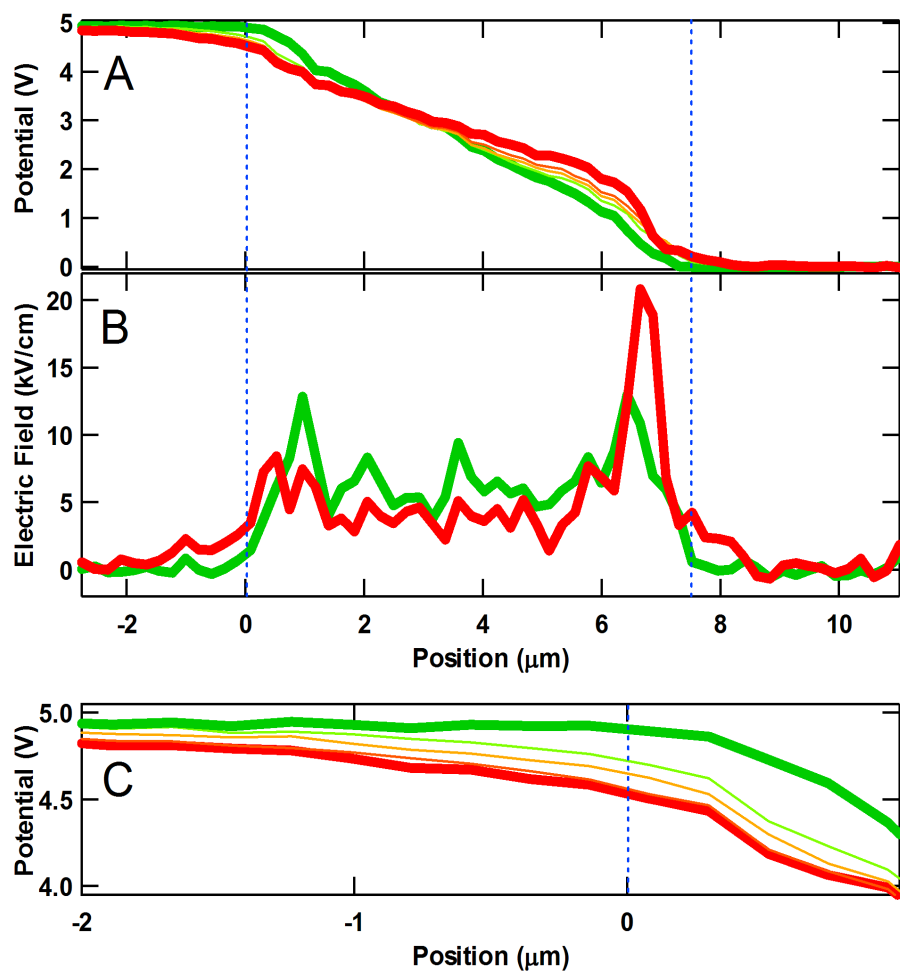


Figure 4.3. (a) Potential across *unpatterned* device. (b) Electric field. (c) Potential near anode.

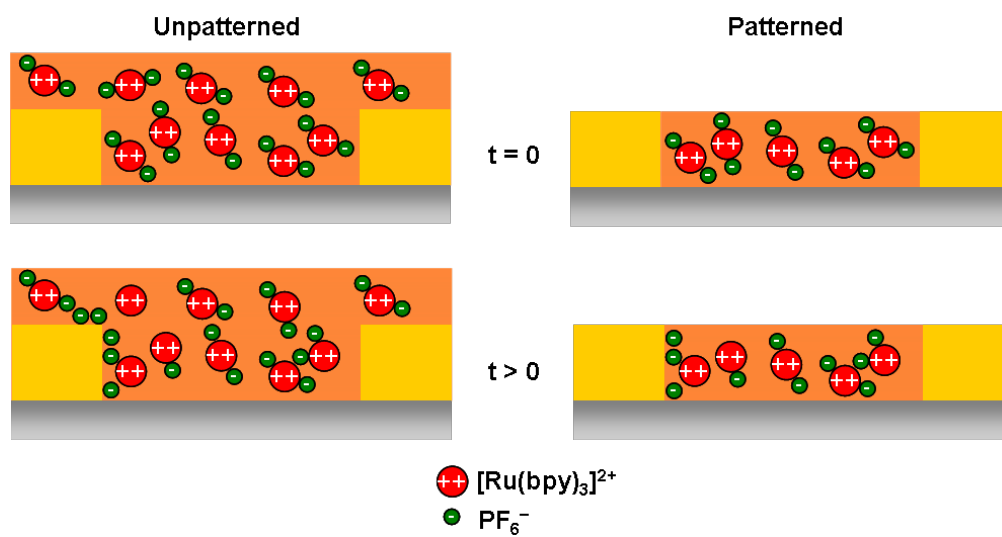


Figure 4.4. Diagram of patterned vs. unpatterned devices under bias.



Under the influence of the applied bias, the counter ions drift towards the anode. However, in the case of a film that extends over the metal electrodes, counter ions that pile up against the anode can diffuse over the electrode. This will result in artificially lower ion concentrations near the electrodes compared with that in sandwich-type devices, where the ions cannot diffuse around the electrode.

This difference in boundary conditions causes measurements on unpatterned planar devices to fail to capture the relevant device physics of iTMCs. It should be noted that the top-contact devices (in which metal electrodes are deposited on top of the  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  film) also suffer from this effect, as ions can diffuse underneath the metal electrodes.

#### ***4.2.5 Patterning Ru(bpy)***

To establish the same boundary conditions as in sandwich-type devices, the  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  layer needs to be patterned to avoid overlap with the metal electrodes, as shown in Figure 4.4. This was achieved by using a variation of the parylene lift-off technique developed by DeFranco et al.[136]. Parylene is a chemical-vapor-deposited polymer that offers conformal, pinhole-free coatings that adhere weakly to a variety of substrates, including freshly cleaned gold[136,137]. Planar devices were prepared using the process shown in Figure 4.5.

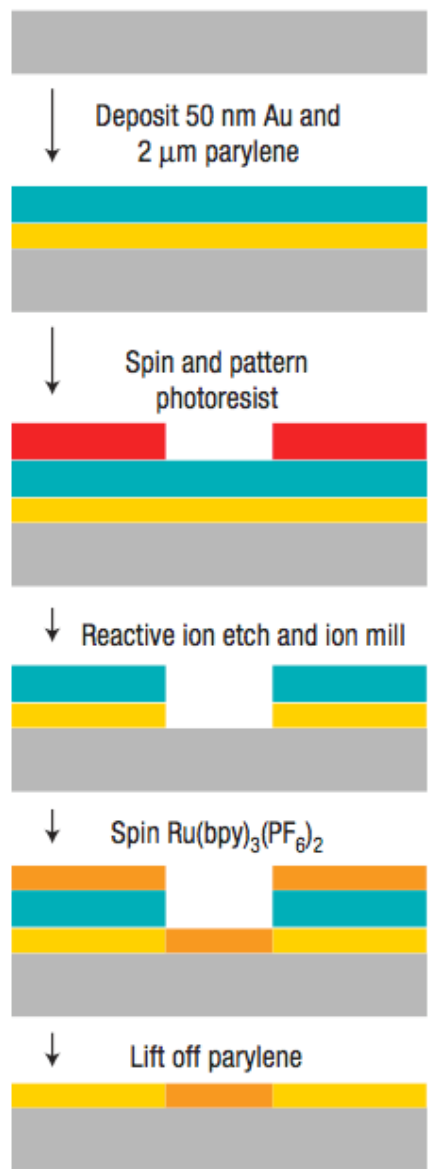


Figure 4.5. Process flow for patterned planar devices.

To fabricate the devices, 500 Å of gold (with a 20–50 Å Cr adhesion layer) was deposited on an oxide-passivated silicon wafer. The gold surface was treated with a surfactant (Micro 90 cleaning solution) to discourage irreversible adhesion of the parylene layer. Approximately 2 µm of parylene C was deposited on the wafer in a PDS 2010 Labcoater. Parylene dimer was vaporized above 80° C (the furnace was kept at 130° C) and then in a separate chamber, the parylene was pyrolysed into the monomer form at 690° C. The sample was held at room temperature so that the parylene polymerized on contact with the surface forming a conformal film. A Shipley SPR 220 3.0 photoresist was spun on at 4,000 rpm and pre-baked at 115° C for 90 s. The device patterns were exposed on a contact aligner and developed after a post-exposure bake at the same time and temperature as the pre-bake.

The parylene layer was etched in an oxygen plasma etcher at 150 W for 12–15 minutes, removing it completely from the gold in the patterned areas. The wafer was then etched in a Veeco ion mill to remove the gold layer underneath. Interdigitated electrode stacks of gold and parylene were left on the wafer. For patterned devices, a dilute solution of  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  (2 mg in 1 ml of acetonitrile) was then spin-cast in a nitrogen glove box onto individual devices at 8,000 rpm, to make a layer of around 200 Å in the channels. The parylene was peeled from the gold, leaving  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  in the channel, but not on top of the electrodes. An illustration of the peeling step is shown in Figure 4.6.

#### ***4.2.6 Measurements of Patterned Devices***

Figure 4.7 shows the distribution of the potential (Figure 4.7(a)) and the electric field (Figure 4.7(b)) in devices with a  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  layer patterned with the technique outlined above. As with the unpatterned devices, the first measurement (thick green trace), shows that the electric field is approximately constant between the two electrodes. After 1 h of continuous application of the 5 V bias, however, a large electric-field enhancement is visible near the cathode, and a smaller field is located near the anode (thick red trace). At the same time, the electric field in the bulk of the device is suppressed from  $5.4 \pm 1.0 \text{ kV cm}^{-1}$  to  $0.9 \pm 0.8 \text{ kV cm}^{-1}$ , a reduction by nearly a factor of 6. A small electric field is also apparent near the anode. A closer inspection (Figure 4.7(c)) shows that the potential over the electrodes is constant, indicating that the patterned samples effectively confine ions between the two electrodes.

#### **4.2.7 Discussion**

The results of Figure 4.7 can be qualitatively understood within the context of the electrodynamic model[104,105]. Under the influence of the applied bias, the  $\text{PF}_6^-$  counter ions pile up against the anode and are depleted near the cathode. The redistribution creates high electric fields at the electrodes, whereas in the rest of the film the field is screened. The interfacial fields assist the injection of holes and electrons, and these carriers move towards opposite contacts primarily by diffusion. A key prediction of the model is that the redistribution of the ionic charge will self-consistently create the highest electric field near the electrode with the highest barrier for charge injection.

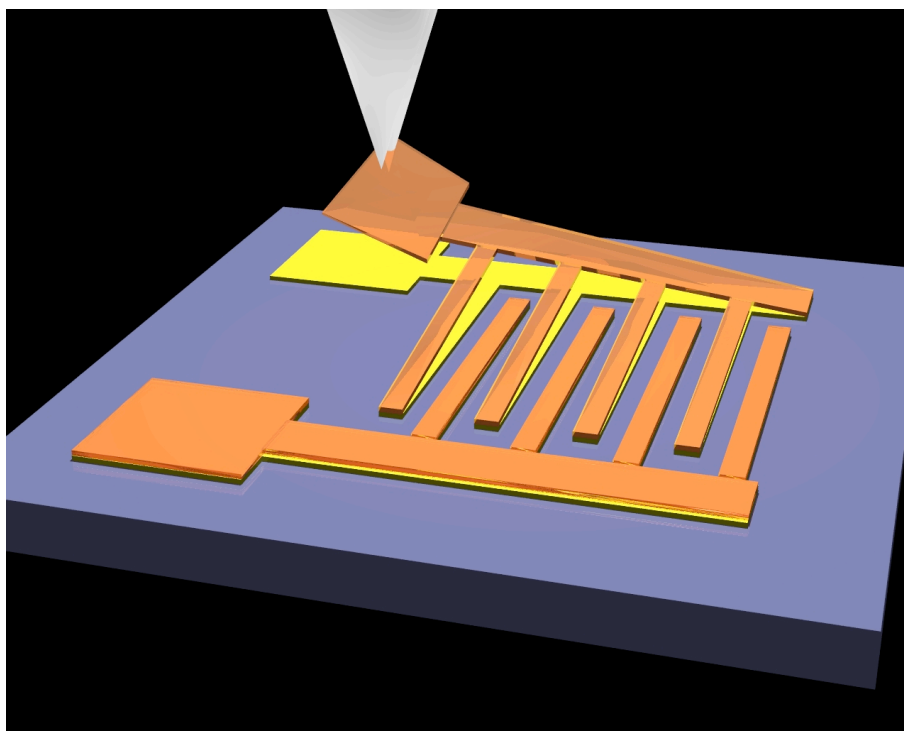


Figure 4.6. Peeling of parylene layer from the electrode with tweezers.

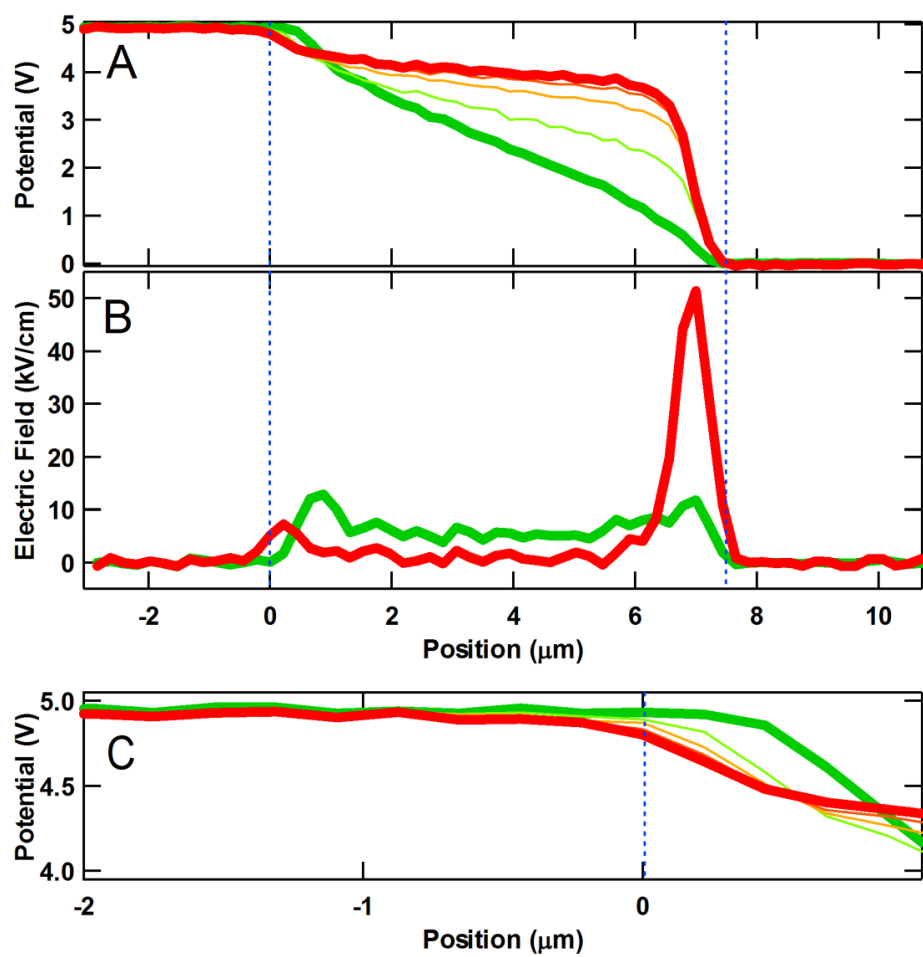


Figure 4.7. (a) Potential across *patterned* device. (b) Electric field. (c) Potential near anode.

As the Fermi level of gold (work function of 5.1 eV) is closer to the HOMO ( $\sim 5.8$  eV) than to the LUMO ( $\sim 3.2$  eV) (ref. 10) of  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$ , a higher barrier is expected for electron injection. As a result, the highest electric field occurs near the cathode.

It should be noted that the problem of bipolar current injection in a semiconductor that contains mobile ions is complicated by the large number of parameters that are needed to account for steric effects associated with ion packing and with injection of electronic carriers across metal–organic interfaces. Rather than aiming at quantitative agreement with the data, the simulations were meant to provide some insight into the physics of LEEC devices with one mobile ion. As a result, the high electric fields predicted by the simulation are chiefly a consequence of the lack of restriction in the density of ions near the electrodes. In real devices, the density of ions near the electrodes will be limited by steric effects, resulting in smaller interfacial fields.

The normalized distributions of potential and electric field in patterned LEECs operating at higher voltages are shown in Figure 4.8 (a, b).

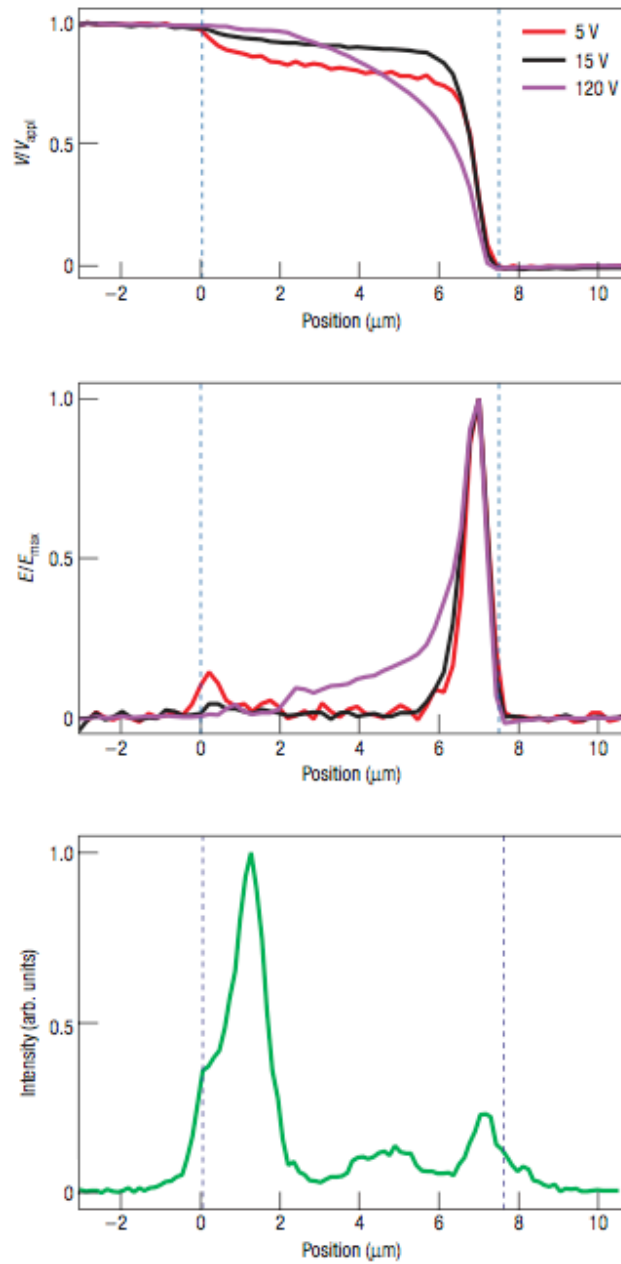


Figure 4.8. (a) Voltage drop at steady state for different applied biases. (b) Electric field. (c) Light emission profile across device. Left side is anode, right side is cathode.



Qualitatively, the general features of 5 V operation are seen in the data for 15 V and 120 V operation (light emission is clearly visible to the eye at the latter voltage). In all three cases, there is a trend towards cancellation of the electric field in the bulk and a drop of the potential near the electrodes. At 120 V, however, some fraction of the potential is distributed over the bulk of the device, leading to an appreciable electric field. This effect is accounted for by the electrodynamic model: at a high applied bias, the ionic space charge is no longer sufficient to screen the field in the bulk[105].

It should be mentioned that the recombination zone in these devices seems to be located near the anode. This was found by mounting a patterned device on an optical microscope and directly imaging its emission with a CCD (charge-coupled device) camera. The data, obtained at a bias of 120 V, are shown in Figure 4.8 (c). The maximum of the emission occurs within less than 2  $\mu\text{m}$  from the anode, whereas a small peak near the cathode is probably due to scattering from the electrode. The location of the maximum was found to remain unchanged as a function of bias down to 30V, the lowest voltage at which emission was still measurable. The location of the recombination zone implies that the hole mobility in  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  is smaller than the one for electrons[105]. Comparison with Figure 4.8 (a, b) shows that there is no significant potential drop near the recombination zone. An alternative interpretation is that the recombination zone corresponds to the small peak at 5  $\mu\text{m}$ , but the light is strongly waveguided in the  $[\text{Ru}(\text{bpy})_3]^{2+}(\text{PF}_6^-)_2$  film and the peaks near the electrodes arise owing to scattering. Again, the majority of the potential drop is away from the recombination zone.

The observation of high interfacial fields, as predicted by the electrodynamic model, has important consequences for the design of LEECs. It explains the ability of these devices to function efficiently even when high-work-function (hence air-stable) cathodes are used. The high-energy barrier at the cathode, which would normally prohibit efficient electron injection, is reduced in width by the interfacial electric field. Smaller counter ions can pack near the electrodes with greater density and produce higher electric fields at the electrodes that help inject electrons and holes more efficiently. On the other hand, if too many ions pile up near an electrode, the resulting electric field will be very high, leading to local electrochemical breakdown of the device. Such phenomena are not only important for LEECs, but for all solid-state ionic devices. EFM measurements on planar and appropriately patterned devices can help to quantify these effects, understand the underlying physics and improve the performance of mixed-conductor devices.

#### ***4.3 Conclusion***

Planar iTMC devices were measured using kelvin probe microscopy in order to measure the ionic distribution during device operation. It was found that unpatterned planar devices had significant drops of voltage on top of the electrodes due to ion migration, leading to an inconclusive result when trying to model a sandwich-type device. Using a novel version of the parylene liftoff technique, material was removed from the top of the electrodes, enabling the direct measurement of the internal fields. The conclusion of the study was that the electrodynamic model best fit the measured fields.



## CHAPTER 5

### ORTHOGONAL PROCESSING USING HIGHLY FLUOROUS SOLVENTS

#### ***5.1 Introduction***

In previous chapters, it has been demonstrated that photolithography may be practiced on organic electronic materials using a parylene interlayer. This gets around the problem of chemical damage and enables both additive and subtractive patterning of a wide range of materials, however with some limitations, which were discussed at the end of Chapter 2. To reiterate: parylene patterning is limited to “open” geometries (designs where the parylene film is continuous across the substrate to allow for peeling), non-overlapping multi-level patterning and substrates from which it can be easily peeled. The reason for the second restriction is that the etch step of the parylene will easily etch through any organic layer underneath, as organic materials are not made to be etch stop layers for oxygen plasma RIE. Thus, a number of devices that would benefit from photolithography, e.g. electrodes patterned on top of OLEDs or OPVs, cannot use the parylene technique in fabrication. Additionally, as will be made clearer in the following chapter, adding additional equipment, especially the use of vacuum deposition, makes for a less appealing technology for commercial purposes. The best approach would be to use photolithographic techniques with no tricks or additional layers, with the same processes as have been established in the industry (LCD or silicon), and with the same equipment.

The research presented in this chapter aims to fulfill these very stringent requirements. Instead of introducing additional protective layers into the process, the

damaging chemicals used in photolithography are substituted for a non-damaging chemistry based on fluoruous solvents. It is demonstrated that these solvents are benign to a wide range of organic electronic materials. Further, photoresists designed to work with these solvents are demonstrated and used to pattern materials and to make working organic electronic devices with novel features.

## ***5.2 Orthogonal Solvents***

### ***5.2.1 Orthogonal Property***

The two extremes of miscibility and orthogonality play a central role in the fabrication of inorganic semiconductor devices. Miscibility allows the removal of layers (by dissolution) when or where they are no longer needed: The wet-etching of various materials with suitable solvents is an example of processes requiring miscibility between the etchant and the target material. Orthogonality, on the other hand, is necessary when a layer deposited from solution must not damage underlying layers. This is the case during the deposition or removal of a photoresist film: The integrity of underlying inorganic electronic materials is not at risk during this process, as their “hard” nature renders them insoluble to the solvents used during photolithographic processing. Leveraging these relationships between materials, silicon electronics has enjoyed great success in scaling devices to smaller and smaller dimensions.

Two solvents are said to be orthogonal to each other if they do not mix in any way. This definition for orthogonality can be seen as analogous to orthogonal vectors, which are defined to have an inner product of zero, so that a material that dissolves well in one type of solvent (vectors are near parallel), is insoluble in another type of

solvent (nearly perpendicular). It is usually not convenient to talk about solvents in this way, because there are only two widely used solvent classes: polar and non-polar.

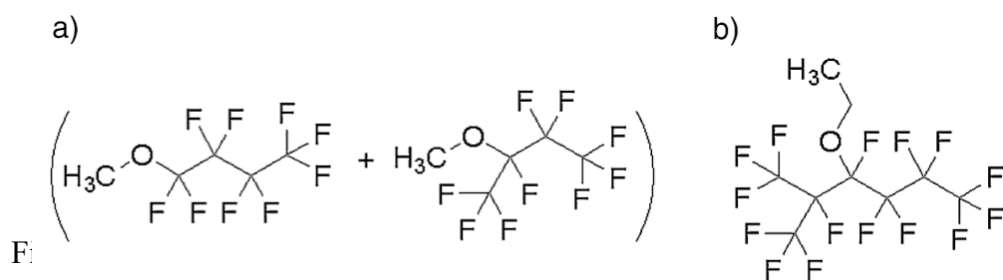
### ***5.2.2 Fluorocarbons as Orthogonal Solvents***

First synthesized and tested as part of the Atomic Energy Project during World War II, fluorocarbons have been found to have unusual properties compared to their hydrocarbon equivalents. Aristid Grosse and George Cady [138] first tested a number of these properties and concluded that in fact these compounds formed the basis of a new field of chemistry the size of, but distinct from, organic chemistry. Fluorocarbons are characterized by a high degree of thermal stability due to the strength of the C–F bond (up to 130 kcal./mol), making the fluorocarbon molecules resistant to cracking even at temperatures above 400°C. They are chemically inert and resistant to oxidation. A lack of hydrogen bonding means that they exhibit very low interaction with oleophilic molecules. In fact, strong interaction only occurs with other fluorinated materials. The properties of fluorocarbons listed above make them a strong candidate for orthogonal processing.

Fluorous solvents are perfluorinated or highly fluorinated liquids, which are typically immiscible with organic solvents and water[139]. Therefore, they naturally extend our options for solvent orthogonality. We chose HFEs out of the variety of other available fluorous solvents since they are well known to be highly environmentally friendly, “green” solvents[140]. HFEs are non-flammable, have zero ozone-depletion potential, low global warming potential and show very low toxicity to humans[140]. HFEs were introduced to industry in 1994 as third generation

hydrofluorocarbon liquids to be used as replacement of chlorofluorocarbons and hydrochlorofluorocarbon refrigerants. HFEs have also been demonstrated as environmental friendly cleaning solvents for electronics[141–143].

Typical commercially available HFEs are isomeric mixtures of methyl nonafluorobutyl ether and methyl nonafluoroisobutyl ether (HFE 7100) and 3-ethoxy-1,1,1,2,3,4,4,5,5,6,6,6- dodecafluoro-2-trifluoromethylhexane (HFE 7500) shown in Figure 5.1.



### 5.2.3 Effect of Hydrofluoroethers on Organic Electronic Devices

We tested the impact of these solvents on well-characterized and commercially available organic electronic materials. The first one was poly(3-hexylthiophene) (P3HT), a prototypical conjugated polymer which is soluble in common non-polar organic solvents such as chlorobenzene and is extensively used in OTFTs.[144] We therefore fabricated a nominally identical batch of P3HT OTFTs and tested them before and after a five minute immersion into a beaker filled with solvent and held at room temperature. In addition to the HFEs listed above, we used representatives of

polar protic (isopropyl alcohol – IPA), polar aprotic (propylene glycol methyl ether acetate – PGMEA), and non-polar (p-xylene) solvents. The second organic electronic material we tested was ruthenium(II) tris(bipyridine) with hexafluorophosphate counter ions  $\{[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2\}$ . This material is an ionic metal complex which is soluble in polar solvents such as acetonitrile and is used in electroluminescent devices. [145] We therefore fabricated a nominally identical batch of  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  electroluminescent devices and tested them after exposure to solvents according to the protocol discussed above.

The results of solvent treatment on device performance are shown in Figure 5.2 and are summarized in Table 5.1. For the P3HT transistors, the transfer characteristics before and after solvent immersion are displayed in Figure 5.2(a).



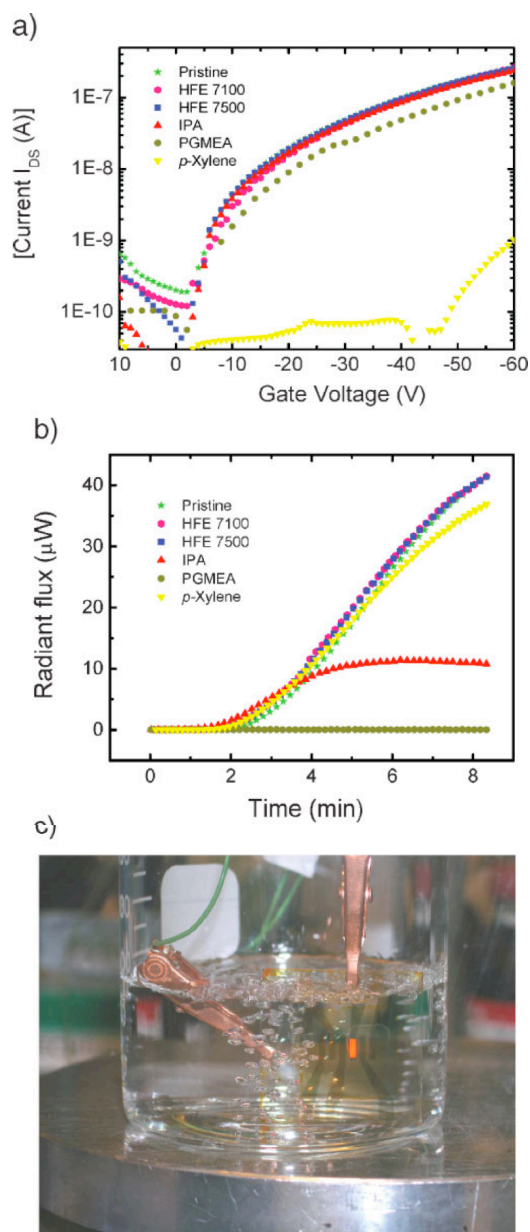


Figure 5.2. (a) Gate sweeps of P3HT devices before and after exposure to solvents. (b) Performance of  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  device with solvent exposure. (c)  $[\text{Ru}(\text{bpy})_3]^{2+} (\text{PF}_6^-)_2$  device operating in boiling HFE solvent.

	Polar		Non-polar	Fluorous	
	Protic IPA	Aprotic PGMEA	p-xylene	HFE 7100	HFE 7500
P3HT	95%	90%	0%	100%	100%
[Ru(bpy) <sub>3</sub> ] <sup>2+</sup> (PF <sub>6</sub> ) <sub>2</sub>	45%	0%	85%	100%	100%

Table 5.1. The results of solvent treatment on P3HT OTFTs and [Ru(bpy)<sub>3</sub>]<sup>2+</sup> (PF<sub>6</sub>)<sub>2</sub> electroluminescent devices. The data represent changes in the field-effect hole mobility of the former and the quantum efficiency of the latter after solvent treatment.

The initial field-effect hole mobility of the OTFTs was  $1.0 \times 10^{-3} \text{ cm}^2/\text{V}\cdot\text{s}$  with a device-to-device variation of 10%. As expected, the transistors fared reasonably well in IPA and PGMEA, showing only a minor decrease in performance. It should be noted that PGMEA, which is extensively used in photolithography, has been utilized in the photolithographic patterning of P3HT and a few other organic materials [146,147].

Immersion in the non-polar p-xylene, however, dissolved the P3HT film and resulted in severe device damage. On the other hand, immersion in the HFEs did not cause any device degradation, indicating that HFEs are excellent orthogonal solvents for P3HT.

Similar results were observed for the [Ru(bpy)<sub>3</sub>]<sup>2+</sup> (PF<sub>6</sub>)<sub>2</sub> electroluminescent devices. Figure 5.2(b) shows the results of solvent treatment in the emission

characteristics of the devices. The emission shows the characteristic delay associated with the redistribution of the PF6<sup>-</sup> counter ions.[145] Table 5.1 shows the resulting loss in device external quantum efficiency upon solvent treatment. As expected, immersion in p-xylene resulted in a rather small loss of performance, while IPA caused a substantial decrease in device efficiency due to an increase in device current, and PGMEA lead to shorting of the devices and complete loss of electroluminescence. Once again, immersion in HFEs did not affect device performance. Therefore, HFEs are shown to be orthogonal solvents for two organic electronic materials with very different polarities, P3HT and [Ru(bpy)<sub>3</sub>]<sup>2+</sup> (PF<sub>6</sub><sup>-</sup>)<sub>2</sub>.

### **5.3 Orthogonal Photoresists**

#### **5.3.1 Calixerene**

In general, materials with higher F content dissolve better in fluoruous solvents. On the other hand, those materials are less adhesive on nonfluorinated surfaces. It is therefore desired to construct a material with a limited degree of fluorination while still exhibiting sufficient solubility and uniform dissolution behavior in HFEs. A design motif was hinted by molecular resists, which are amorphous small molecules with a monodisperse molecular weight distribution. Recently we have reported that a resorcinarene material shows excellent patterning properties under conventional lithographic conditions[148]. The same molecular framework was adopted, to which four semiperfluoroalkyl chains and eight acid-cleavable *tert*-butoxycarbonyl (*t*-Boc) groups were appended. The resulting resorcinarene **6** in Figure 5.3 had 36% F content by weight. Resorcinarene **6** is able to form a negative tone image by transformation into

an insoluble form upon an acid-catalyzed deprotection reaction, in which  $H^+$  is liberated from the photoacid generator (PAG) under UV exposure (Figure 5.3) [149,150].

Synthesis of the resorcinarene **6** began with the alkylation of 4-hydroxybenzaldehyde **1** with the semiperfluoroalkyl iodide **2**[151]. The recrystallized product **3** was then reacted with an equimolar amount of resorcinol under acidic conditions.<sup>19</sup> The resorcinarene **5**, which is only sparingly soluble in THF, was recovered as a fine, pale-yellow powder in high yield.



Size exclusion chromatography showed that the product **5** is composed mainly of two compounds, one with  $M_n$  ) 2500 and the other with  $M_n$  ) 1700 compared to the polystyrene standard (Supporting Information). It is believed that those two are stereoisomers which have different hydrodynamic volumes[152]. The presence of stereoisomers stabilizes the amorphous state of the resorcinarene **6**, which would enable quality film formation (XRD data in Supporting Information). *t*-Boc protection of the eight hydroxyl groups in the resorcinarene **5** was completed in a mixed solvent of THF and benzotrifluoride. Thermogravimetric analysis (TGA) and differential scanning calorimetry (DSC) showed that resorcinarene **6** is stable up to 150° C and undergoes glass transition at 82° C. Solubility tests confirmed that resorcinarene **6** is moderately soluble in HFE-7200.

Lithographic evaluation began with spin-coating films of the resorcinarene **6** and PAG mixture on various substrates. The PAG **7** [Figure 5.4(a)] was employed because of its good sensitivity under UV ( $\lambda$  ) 365 nm) exposure conditions[153]. Uniform films were cast on Si, glass, and polyimide-coated wafers from a solution in HFE- 7500 (4 parts by vol.) mixed with a small amount of propylene glycol methyl ether acetate (1 part by vol.). Following UV exposure (84 mJ/cm<sup>2</sup> with Si substrate), bake (at 70 °C), and development in HFE-7200, at least 600 nm features were generated on the aforementioned substrates [Figure 5.4 (b, c)]. Under electron-beam exposure conditions, 80 nm patterns could be achieved without extensive optimization [Figure 5.4 (d)], which demonstrates that lithography employing HFEs can be a useful tool to realize sub- 100 nm features.

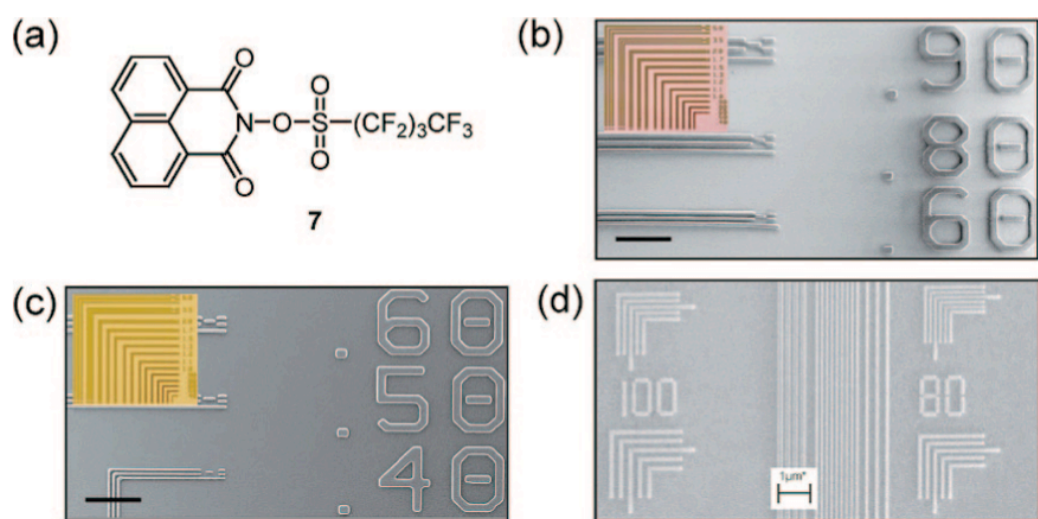


Figure 5.4. (a) Schematic of PAG. (b, c) Images from optical lithography. (d) E-beam patterns.

### 5.3.2 *FDMA-NBMA*

Poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) is a mechanically flexible, transparent, and highly conductive polymer blend, which has found various applications in organic electronics including serving as the electrode material for plastic substrates, because of its low-temperature processing requirements, and as charge-injection/-extraction layers in OLEDs and photovoltaic devices.[154–156] However, photolithographic patterning of PEDOT:PSS for device components is not straightforward, because i) PEDOT:PSS films are damaged by aqueous solutions, which are standard developers in conventional photolithography, and ii) acid-sensitive photoresists are adversely affected by the acidic PEDOT:PSS.

In designing a HFE-compatible photoresist, it was most important that the photoresist be soluble in fluoruous solvents. In general, fluoruous solvents dissolve highly fluorinated materials.[157] The copolymer, derived from the highly fluorinated monomer and photolabile monomer, was expected to yield a material that exhibits a solubility switch following UV irradiation.[158,159] The photolabile component, the ester of 2-nitrobenzyl alcohol and methacrylic acid, decomposes under UV exposure to yield a carboxylic acid and nitrosobenzaldehyde.[23] The resulting polymer is no longer soluble in HFEs. Following the development in HFEs, the still-soluble unexposed regions are washed away to leave the insoluble exposed area as a negative-tone image.



The two monomers were randomly copolymerized by radical initiation using 2,20-azobis(2-methylpropionitrile) (AIBN). Multiple polymers were synthesized with varying compositions. Polymers that lacked sufficient incorporation of the fluorinated monomer proved insoluble in HFEs. Conversely, polymers without sufficient incorporation of the photosensitive monomer proved unpatternable. The compositions of the two monomers were varied to obtain optimum photosensitivity while still retaining enough fluorination to allow processing in HFEs.

To demonstrate patterning properties, polymer was lithographically evaluated on both silicon (Si) and glass substrates. The photoresist was spin-coated from HFE-7600 and then patterned under 248 and 365 nm UV exposure conditions. Pattern development was carried out in HFE-7200. Figure 5.5 shows well-resolved sub-micrometer lines on Si and glass. Notably, this photoresist is soluble in HFEs without cosolvents, and all processing steps are achieved through HFEs.

Sensitivity profiles were obtained for the polymer at both 248 and 365nm. The polymer exhibits very different sensitivities at different wavelengths. At 248 nm, the dose is 84 mJ/cm<sup>2</sup>, whereas at 365nm, the dose is 2700 mJ/cm<sup>2</sup>. However, this behavior is expected, as the nitrobenzyl group is likely to undergo faster decomposition by the irradiation of high-energy photons.[160]

To further explore the patterning properties, the photoresist was also patterned under electron-beam (e-beam) exposure conditions. Well-resolved lines down to 100 nm were obtained, as shown in Figure 5.5(d).

It should be emphasized that the photosensitive monomer was carefully selected to enable nonchemically amplified patterning; an imaging mechanism that does not rely on acid-catalyzed deprotection reactions.[161] The advantages of this pathway are substantial, in particular for the patterning of PEDOT:PSS films. PEDOT:PSS is a difficult material to pattern with acid-sensitive photoresists (photoresists that require a photoacid generator), in that PEDOT:PSS itself, being highly acidic, can decompose the resist. Typically, following patterning with a chemically amplified resist, a thin layer (~10–20 nm) of decomposed photoresist is left on the PEDOT:PSS interface. [158,162]

Preliminary studies on PEDOT:PSS patterning were first carried out with our acid-stable photoresist. PEDOT:PSS was spin-coated onto an Si wafer in a thin film. The polymer was then applied and subsequently removed. Before-and-after measurements showed that the thickness of the PEDOT:PSS film remains exactly the same (51nm), indicating no resist decomposition. Similarly, PEDOT:PSS was spun-cast, followed by photoresist application. The photoresist was then flood exposed with 248 nm UV light and subsequently removed. Before-and-after thickness measurements again show the PEDOT:PSS film unchanged (51 nm). Therefore, no residual layers of decomposed resist were found, as with chemically amplified resists. The PEDOT:PSS interface is left clean and unaffected following resist removal.

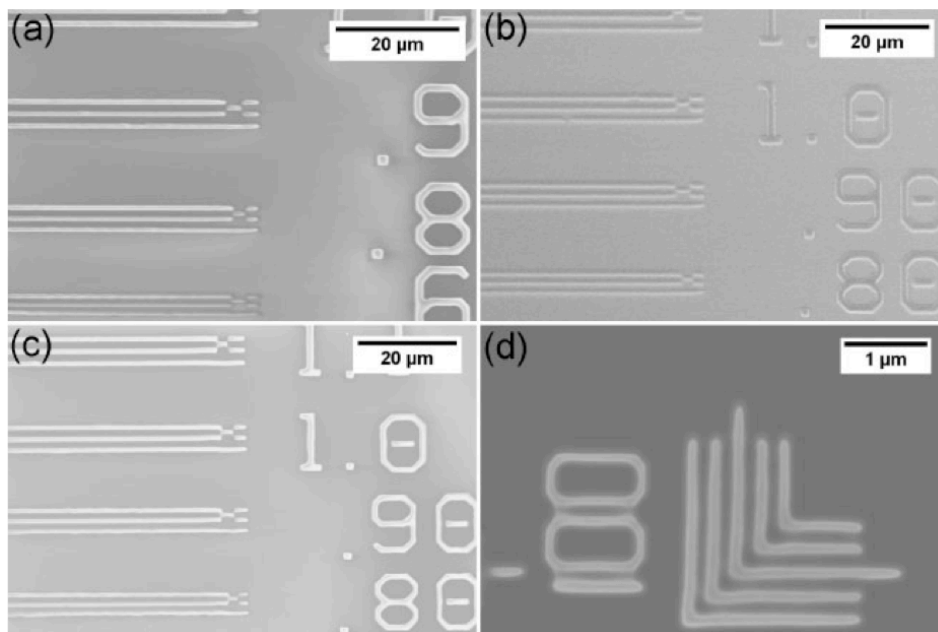


Figure 5.5. (a–c) Lithographic patterns in FDMA-NBMA. (d) E-beam patterns.

#### ***5.4 Conclusions***

A novel approach to patterning organic electronic materials was demonstrated. By changing the chemistry used in photolithography from one with organic solvents and aqueous bases to one using fluoruous solvents, the damaging aspects of the process can be mitigated. Two photoresist materials were developed and demonstrated. Calixerene is a chemically amplified molecular glass resist, while the random co-polymer FDMA-NBMA is a non-chemically amplified resist. Both negative tone resists can be used on a wide range of organic materials, with FDMA-NBMA being specifically designed to work with acidic materials such as PEDOT:PSS.



## CHAPTER 6

### OTFT DEVICES AND CIRCUITS

#### ***6.1 Introduction***

In the previous chapter, the concept of orthogonal processing was introduced and two photoresist systems were demonstrated that work exclusively with fluororous chemistry to make patterns. In this chapter, those systems are applied to OTFTs, to make high-performance transistors and circuits using photolithography exclusively. It is here that the power of using photolithography directly on organic materials can be appreciated, compared with the difficulties that arise using indirect techniques such as parylene patterning.

First, it is shown that orthogonal lithography can be used to pattern metals on top of organic materials, allowing for photolithographically patterned top contact transistors to be made for the first time. This technique is then extended to make ring oscillator circuits where every level is patterned using photolithography, including the organic layer and top contact source-drain electrodes. From these examples, it can be seen that orthogonal processing is a feasible industrial process that can be used to make all manners of organic circuits, as well as many other interesting and unique devices.

#### ***6.2 Applications to Organic Transistors***

##### **6.2.1 Top Contact vs. Bottom Contact OTFT Architectures**

The different types of OTFT architecture arise from a different ordering of the layers. Four standard variations exist and of those four, two are most commonly used. The OTFT can be bottom gated or top gated and have bottom or top contacts in any combination, yielding four possibilities. In top gated architectures, the gate dielectric and gate electrode layers are deposited (no native oxides exist as they do in silicon) on top of the organic layer. The advantage is that application of the dielectric can also serve as an encapsulation layer, not inconsiderable since most organic semiconductors are unstable in air and moisture. Still, top gated OTFTs are usually not done for two reasons. First is that special care must be taken to assure that no damage is done in the dielectric deposition process (the dielectric usually protects the underlying layers during the gate deposition step), and this can be severely limiting, since only low temperature processes without or with non-damaging solvents may be used. It has nonetheless been demonstrated with materials such as polyvinyl alcohol (PVA), parylene and various oxides deposited by atomic layer deposition (ALD). The other potential problem is that many organic films have rough surfaces, which can lead to poor transport and wildly varying fields at the interface in the case of non-conformal dielectric coatings. Polymer OTFTs with inkjet printed layers use top gate architectures more than OTFTs based on vacuum deposited small molecules.

Bottom gated devices are far more common. A highly doped silicon wafers with thermally grown oxide often serves as the gate and gate dielectric, respectively. For bottom contact transistors, the source and drain electrodes are patterned first before the active layer is deposited and patterned (or not). Photolithography is often used to

define these electrodes, because it is both reproducible and can make small channels for higher transistor performance. Since the organic layer goes on later, the resist chemicals pose no threat as long as the water used in the development stage is driven off of the wafer afterwards. Top contact devices pattern the electrodes on top of the organic layer. Since resist processing chemicals can damage the underlying layers in this case, alternate methods must be used to pattern the electrodes. The most popular way to do this is through the use of a shadow mask. A shadow mask is simply a thin metal sheet with holes etched into it. The shadow mask is placed flush with the substrate and metal is evaporated through the mask, producing patterns only where the holes appear. Depending on the distance between the mask and the substrate, the patterns may be larger than the size of the holes due to spreading. Typical minimum feature sizes are around 20 $\mu\text{m}$  because of this limitation and because it is difficult to etch very small holes in metal that is itself several mils thick. Spreading can also cause ill-defined interfaces where a small amount of metal migrates into the channel in an uncontrolled way, sometimes causing shorts. The advantage is that a very clean interface is made between the metal and the organic layer, because the metal hasn't had time to build up an oxide or (more commonly with the noble metals such as gold and platinum) an organic scum layer from sitting in air.

The biggest difference in performance, however, is that many organic materials do not form high quality films on substrates with electrodes already on them. Pentacene is a particularly good example of this phenomenon. Pentacene grown on a smooth surface a low rate will form large grains that provide good transport reflected in high



field-effect mobilities ( $\mu$ ). The individual molecules have a low attraction to the surface, so they stand up and form the large grains. On gold, pentacene has a large interaction and tends to lie down. The result is that pentacene in the channel has a different morphology from pentacene on the electrodes. Smaller grains form near the electrode edge because of heterogeneous nucleation and voids can also occur at the edge. In the case of pentacene, the problem can be addressed by treating the gold electrodes with a thiol-terminated SAM layer that allows grains to grow continuously onto the electrodes [163].

In general, the tradeoff between top and bottom contact architectures is between good extrinsic parameters—channel length, critical dimension control—and good intrinsic parameters—mobility and charge injection—that don't depend on geometries.

By allowing electrodes to be photolithographically patterned on top of the organic layer, orthogonal processing will allow the best of both worlds: top contact performance with bottom contact channel lengths.

### 6.2.2 Experimental

Highly-doped silicon wafers with a thermally-grown 360 nm SiO<sub>2</sub> layer were used as substrates. They were cleaned in isopropanol and acetone and treated with hexamethyldisilazane (HMDS). Pentacene films were deposited onto these substrates at a rate of 0.1 Ås<sup>-1</sup> and a pressure of 5 x 10<sup>-7</sup> Torr. 200 Å thick films were deposited, as determined by a quartz crystal monitor. Resist solutions were prepared by mixing R<sub>F</sub>-Calix-*t*Boc powder (15 wt%) with HFE 7500, using a small amount of propylene glycol methyl ether acetate (PGMEA) as co-solvent. A photoacid generator (PAG, *N*-

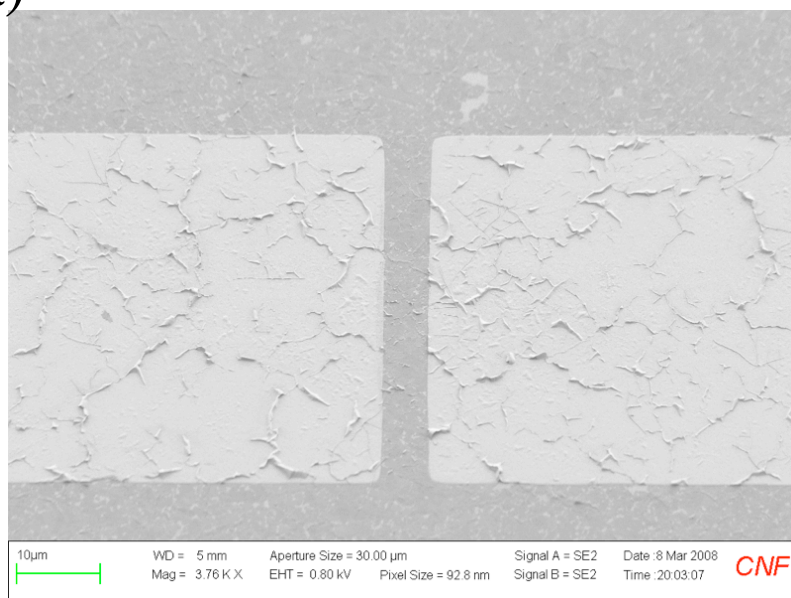
*nonafluorobutanesulfonyloxy-1,8-naphthalimide*, 0.5 wt%) was mixed into the solution and the solution was filtered through a syringe filter (nylon, 0.20  $\mu\text{m}$ ). After deposition of pentacene, the wafer was removed from the glove box, where a resorcinarene resist solution was spin-coated onto the wafer at 1000 rpm. Patterns were then exposed on a GCA Autostep ( $\lambda=365$  nm). The film went through post-exposure bake at 70°C for 30 seconds and was developed in HFE 7200. After development, a layer of 50 nm thick gold was deposited to form the source and drain contacts. Finally, the resist film was lifted off in ethanol (5 vol%)-HFE 7100 mixture to leave patterned gold electrodes on top of the pentacene film.

### 6.2.3 Results

We successfully fabricated top contact transistors with 1  $\mu\text{m}$  channel lengths using pentacene, as shown in Figure 6.1. Pentacene film growth is known to be particularly sensitive to substrate roughness, which makes top contact devices show superior performance in comparison to bottom contact devices[164].

The field effect mobility of the photolithographically fabricated pentacene transistor was found to be  $0.45 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . This is a similar field-effect mobility (but at a smaller channel length) than in transistors made by vacuum deposition of metal through a shadow mask.

(a)



(b)

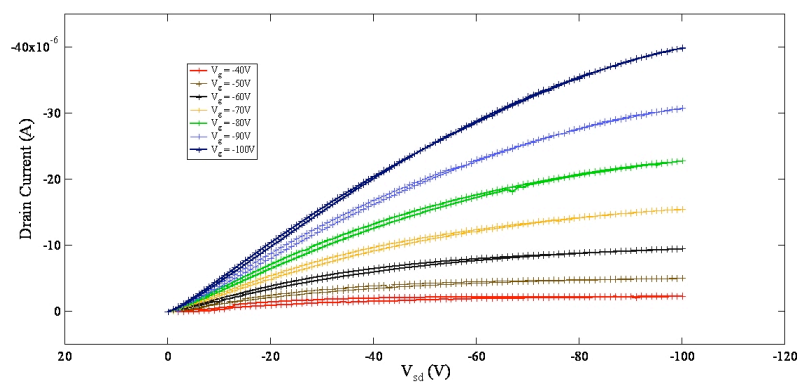


Figure 6.1. (a) Top source-drain electrodes on pentacene. (b) IV curve.

#### **6.2.4 Discussion**

The mobility is much improved in these devices compared with the transistors of the same dimensions shown in Chapter 3. The top-contact geometry helps quite a bit in getting nice, large crystal grains without having electrodes break up the domains or nucleate smaller grains at the edges. The IV curve does again show some injection limitations, perhaps from residue left over after developing the resist.

#### **6.3 Ring Oscillator Circuits**

A ring oscillator comprises an odd number of inverter circuit elements linked in series. Changing the supply voltage changes the delay through each inverter, with higher voltages typically decreasing the delay and increasing the oscillator frequency. Beyond demonstrating individual device performance, a good test of a patterning process is often to make more complex circuits. A ring oscillator is a circuit that outputs a sinusoidal wave with a DC voltage as the only input (other than ground).

Ring oscillators are useful for demonstrating a new patterning technique since they have some meaningful amount of complexity, require multiple transistors to operate together, thus showing reproducibility, demonstrate patterning on every level and have an easily understood figure of merit: output frequency. Ring oscillators aren't just for show, however. Many circuits require an internal oscillating source. The phase locked loop, used in radio tuning and digital timing, is a good example.

The faster each individual transistor saturates (the term used is stage delay), the higher the frequency of the output signal. Applying a higher voltage will increase both the output amplitude and frequency; so the higher the voltage the device can withstand

before failing, the better the output obtainable. The devices are usually limited by thermal breakdown or current punch-through of the gate oxide.

### **6.3.1 Smooth Gold for Gate Electrodes**

Patterned gate electrodes are required for circuits such as the ring oscillator. Since the substrate can no longer be used as a gate, some suitable substitute must be used, such as metal. The downside to using a patterned metal gate is that it is difficult to obtain the smoothness required for good device parameters. Pentacene in particular is sensitive to surface roughness. Typical roughness of thermal oxide on a silicon wafer is on the order of 2Å RMS.

In order to make the surface as smooth as possible for the pentacene deposition step, the gate electrode was made of gold using a mercapto-silane monolayer for adhesion. The method has been used by Mahapatro et al. to make nearly atomically flat gold films for molecular electronics applications[165]. Our own efforts were able to achieve gold surfaces with RMS roughness of 6–7Å. First a test grade silicon wafer was oxidized to form a 500nm passivation layer of SiO<sub>2</sub>. The wafer was cleaned in a hot piranha solution. It was then exposed to oxygen plasma for 10 minutes and dipped in HCl and DI water for ten minutes. Immediately after this cleaning and surface preparation procedure, the wafer was placed in an MVD 100 tool where it was coated with a monolayer of MPTMS.

### **6.3.2 Al<sub>2</sub>O<sub>3</sub> Gate Dielectrics Deposited by ALD**

Dielectric deposition and patterning represent another problem area for organic circuits. After obtaining smooth gate metal, it is important to use a dielectric material

that is itself smooth. It is also desirable to have a thin, high-k dielectric layer so that the voltage needed to drive the ring oscillator is low and the fields in the transistor are high, improving mobility and switching speed.

Atomic layer deposition is a process by which very thin conformal layers of material (most often oxide materials) are deposited using a binary chemical reaction. In case of  $\text{Al}_2\text{O}_3$ , the chamber is saturated with tetramethyl aluminum (TMA). Only a monolayer of TMA can form because it doesn't stick to itself. Thus the process is self-terminating. A second chemical, water, is allowed to react with the TMA layer in the presence of a plasma field or using thermal effects to complete the reaction. A monolayer of  $\text{Al}_2\text{O}_3$  is deposited in this way. By repeating the process a certain number of times, an oxide layer can be deposited with Ångström level control. The process is also conformal, coating deep into crevices, with a high degree of uniformity. ALD can be done at temperatures from around 110°C up to 400°C. Higher quality films are obtained at higher temperatures, since this ensures that all reactant byproducts are driven from the film, leaving it denser and more resistant to electrical breakdown. For this experiment, all films were deposited at 110°C, in part to avoid affecting the MPTMS attached gold layer. For the same reason, plasma enhanced deposition was avoided.

Figure 6.2 shows an AFM image of the resulting film on the smooth gold from the previous section. Roughness was kept at around the same level of 0.6 Å rms, although the polycrystallinity of the  $\text{Al}_2\text{O}_3$  film can be observed in the image.

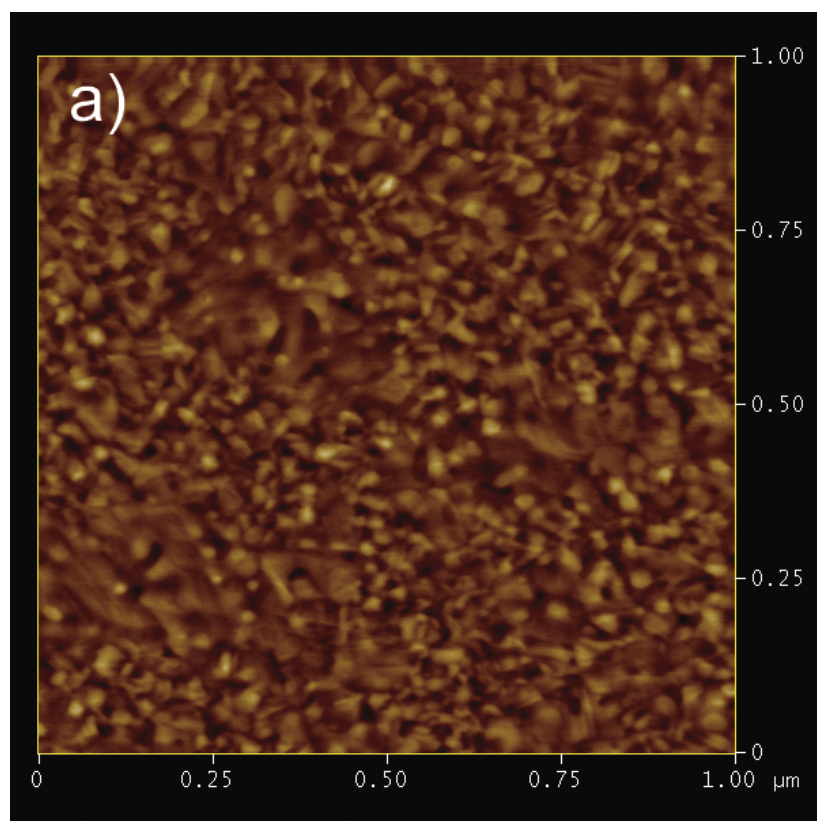


Figure 6.2. AFM of gold surface with an RMS roughness of 0.7 nm.

Film thickness was determined using the Woolam ellipsometer. Four hundred forty loops were used to deposit 60nm of  $\text{Al}_2\text{O}_3$  on top of gold. The same film thickness was measured on top of  $\text{SiO}_2$ . Breakdown voltage varied between XV and YV, giving a breakdown field of X–Y V/cm<sup>2</sup>.

### **6.3.3 Pentacene Transistors Using Thin $\text{Al}_2\text{O}_3$ Gate Dielectric**

In order to test the performance of standard transistors on an  $\text{Al}_2\text{O}_3$  layer, a 60nm film was deposited on a highly doped silicon wafer under the conditions described above.

Pentacene was thermally deposited onto the substrate at a rate of 0.1Å/s until a thickness of 30nm was reached with the substrate held at 60° C to enhance crystallinity. The mobility of the device was extracted from the gate sweep with the source and drain held at 20V (saturation conditions). This device yielded a field-effect mobility of 1.5cm<sup>2</sup>/V•s, higher than is typical in our lab.

### **6.3.4 Design and Fabrication Considerations**

Ring oscillators were fabricated in order to demonstrate multi-layer patterning using photolithography only. The devices consisted of four separately patterned layers, the first two of which, the gate metal and gate dielectric layers, were patterned using standard DNQ-Novalak resists. Both the active (pentacene) layers and top contact source/drain electrodes were made using the resorcinarene resist and fluororous developer.

Smooth gold was deposited in the manner explained above. After the monolayer was in place, 500Å of gold was deposited onto the substrate at a rate of 0.5Å/s using e-beam deposition at a pressure of  $1 \times 10^{-6}$  Torr. The films were measured on a Digital



Instruments AFM to determine surface roughness. The gate electrode patterns were formed using a wet etch (KI/I<sub>2</sub>) using SPR220 3.0 resist exposed on a GCA i-line stepper as an etch mask.

A conformal coating of Al<sub>2</sub>O<sub>3</sub> was deposited using atomic layer deposition (ALD) on an Oxford ALD tool. ALD uses self-terminating surface reactions to deposited thin films a single monolayer at a time. The depositions took place at 110°C using a thermal process. Sixty nanometers of Al<sub>2</sub>O<sub>3</sub> was deposited on top of the gate electrodes. Patterning the dielectric layer was also accomplished using a wet etch process, with the same tools as the gate electrode layer. Aluminum etchant type A (phosphoric acid, nitric acid, acetic acid) was used to etch the dielectric layer.

Pentacene was deposited onto the substrate at a rate of 0.1 Å/s and a pressure of 5 x 10<sup>-7</sup> Torr. Average layer thicknesses of 200Å were deposited, as determined by a crystal monitor. Resist solution was prepared by mixing 10 wt% resorcinarene powder with HFE 7500, using a small amount of PGMEA as co-solvent. A photoacid generator (PAG, 0.5 wt%) was mixed into the solution and the solution was filtered to remove impurities. After deposition of pentacene, the wafer was removed from the glove box, where resorcinarene resist was spin-coated onto the wafer at 2000rpm, making a film approximately 300nm thick. Patterns were exposed on the GCA Autostep. The film went through post-exposure bake of 70°C for 30 seconds and was developed in HFE 7200. The unprotected pentacene was etched in oxygen plasma for 30 seconds and the resist was removed with HFE solvent.

Source/drain electrodes were patterned using a liftoff method. After development of the resorcinarene resist, a layer of 500Å thick gold was deposited on top of the pentacene to form the contacts.

### 6.3.5 Results

In order to prove the process at a higher-level *vertical integration*, we fabricated ring oscillators based on 1 µm channel length pentacene OTFTs (Figure 6.3). The device consisted in four vertical photolithographically patterned layers, with the top two layers being patterned using orthogonal photolithography. Other layers were fabricated using standard techniques with DNQ-novolac resists. Fabrication details can be found in the supplemental materials section. The devices exhibited a turn on voltage of 10–15V and had a peak frequency of 18 kHz at 55V of applied bias. The gate delay of the five-stage ring oscillator is 5.5µs.

### 6.3.6 Discussion

This performance compares favourably to OTFT-based ring oscillators made with other methods[166]. The speed of the devices is increased by precise alignment of the gate electrode with the channel, minimizing parasitic capacitance. Increasing the mobility of the transistor material would, of course, have a commensurate impact on frequency. The devices were fairly reproducible for a lab environment, with >90% of tested oscillators functioning properly.

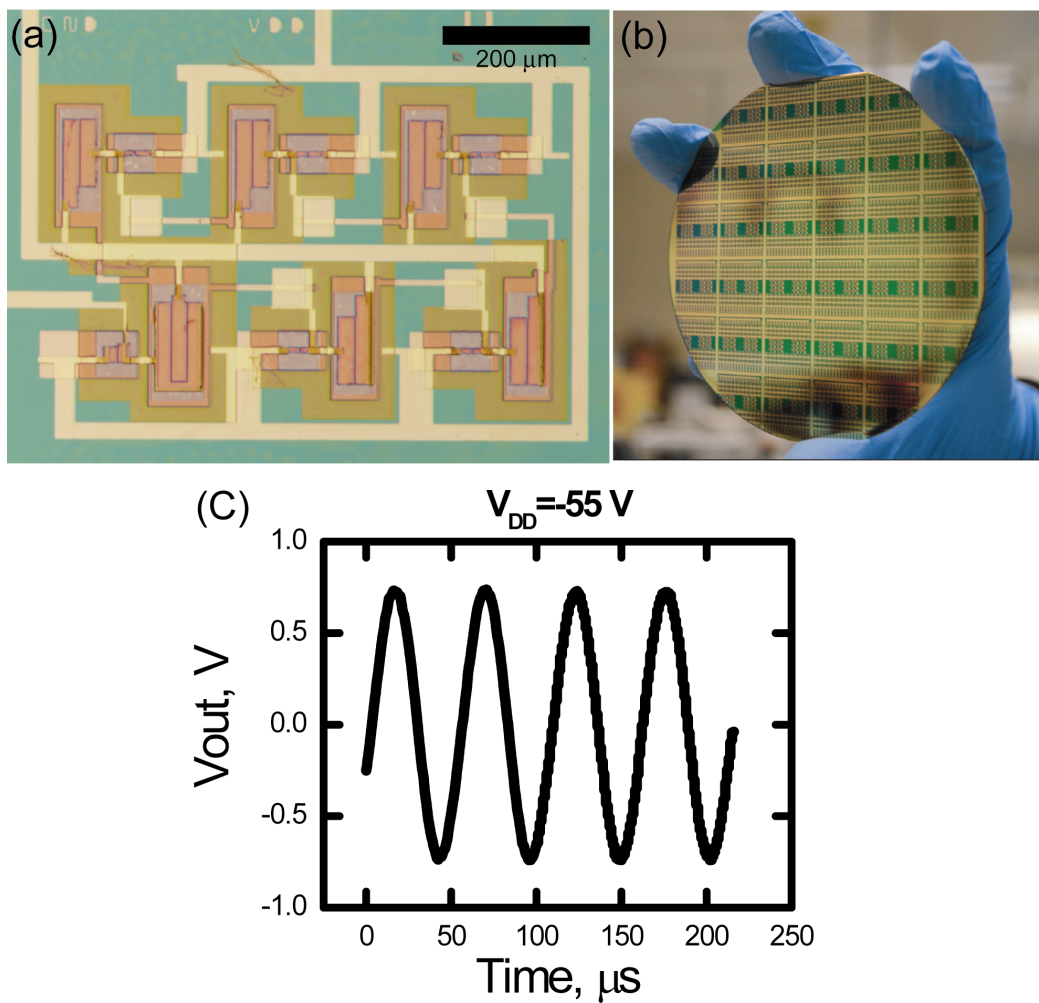


Figure 6.3. Ring oscillator based in 1  $\mu\text{m}$  long channel Pentacene OTFTs. (A) Optical microcopy image of ring oscillator based on Pentacene TFTs. (B) Output characteristic of the device at  $V_{\text{DD}} = -55 \text{ V}$ .

#### ***6.4 Conclusion***

Orthogonal processing has been successfully applied to OTFT devices and circuits, demonstrating its potential for commercial application in high-volume manufacturing. Particularly encouraging is the fact that the entire process was done using standard cleanroom equipment, as are widely available worldwide, in both IC manufacturing environments as well as flat panel display manufacturers. An effective process such as this one may be readily adopted to make organic or hybrid circuits on existing infrastructure and finally make organic electronics a commercial reality.



## CHAPTER 7

### SUMMARY OF CONCLUSIONS

The ultimate goal of this research was to allow the broad range of patterning and processing tools used to make all of the world's electronics applicable to the world of organic electronics. To this end, care was taken to find techniques and methods that would avoid unnecessary complications in applying photolithography and plasma etching to organic materials to make a variety of devices. Because a general method was developed with this research, new opportunities for unique and interesting devices are available to other researchers. It is also possible that some of the techniques used here will enable organic electronics to be manufactured on a large scale, alongside their inorganic brethren.

Along with developing these techniques, some fundamental problems have been addressed. In particular, new insight has been made on the mechanisms responsible for making iTMCs operate, and from this new breakthroughs in solid-state lighting may be possible.

Finally, the use of orthogonal processing to allow for direct patterning of organic materials with photolithography is an important development, but it also opens up a rich vein of other research, by expanding on the possibilities for finding orthogonal chemistries for a wide range of problems outside of this field. It is my hope that these paths lead to somewhere interesting.

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